

EE 330

Lecture 6

- Basic Logic Circuits
- Complex Logic Gates
- Pass Transistor Logic

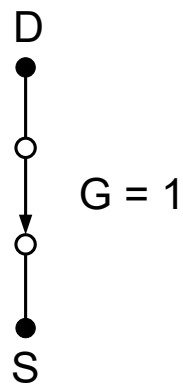
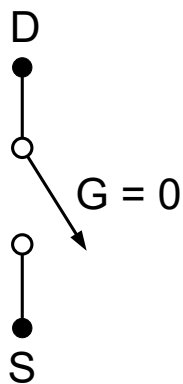
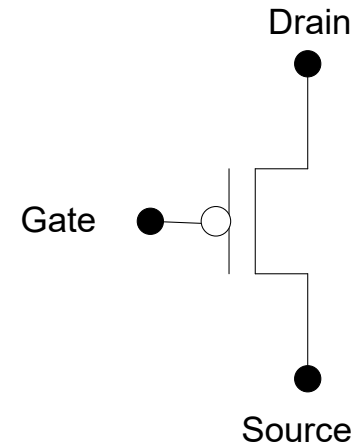
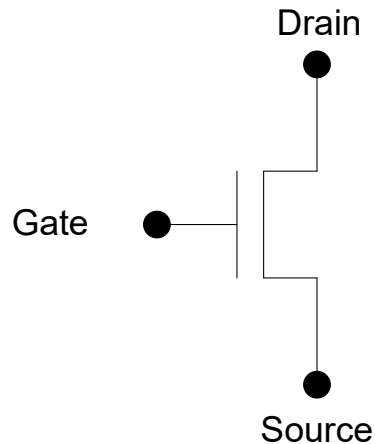
Models of Devices

- Several models of the electronic devices will be introduced throughout the course
 - Complexity
 - Accuracy
 - Insight
 - Application
- Will use the simplest model that can provide acceptable results for any given application

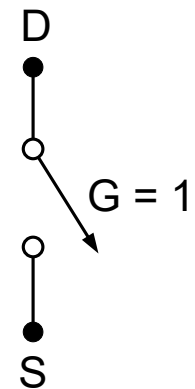
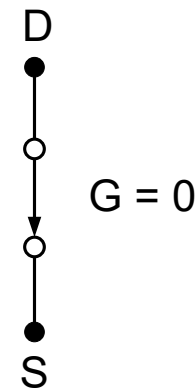
Review from Last Time

MOS Transistor

Comparison of Operation



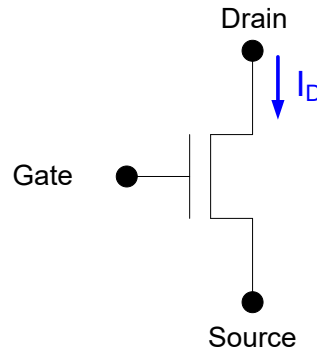
Source assumed connected to (or close to) ground



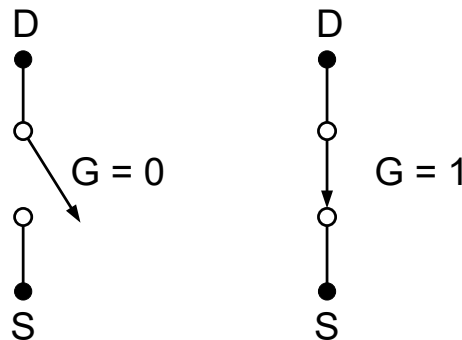
Source assumed connected to (or close to) positive V_{DD} and Boolean G at gate is relative to ground

Review from Last Time

MOS Transistor MODEL



Equivalent Circuit for n-channel MOSFET with source at ground

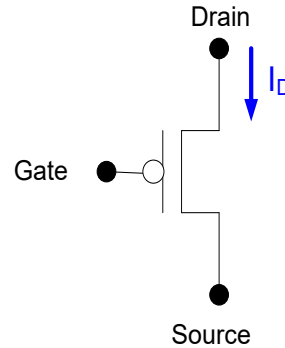


Mathematical model (not dependent upon Boolean notation):

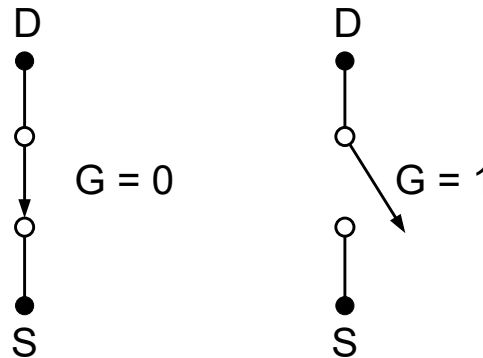
$I_D = 0$	if V_{GS} is low (or negative)
$V_{DS} = 0$	if V_{GS} is high

Review from Last Time

MOS Transistor MODEL



Equivalent Circuit for p-channel MOSFET with Source at VDD



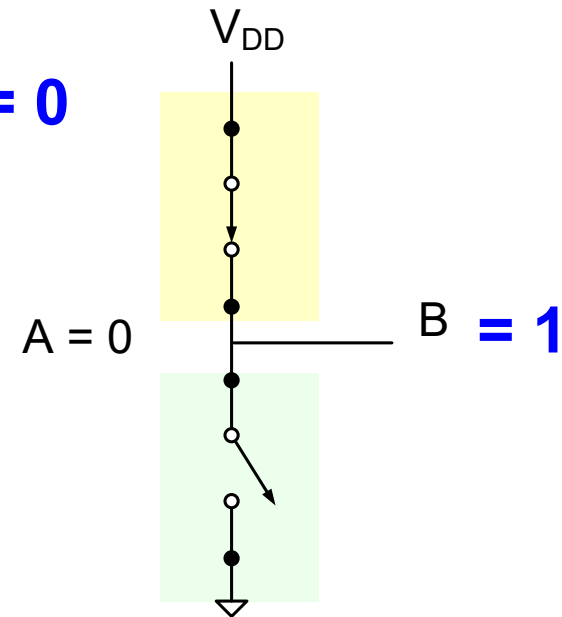
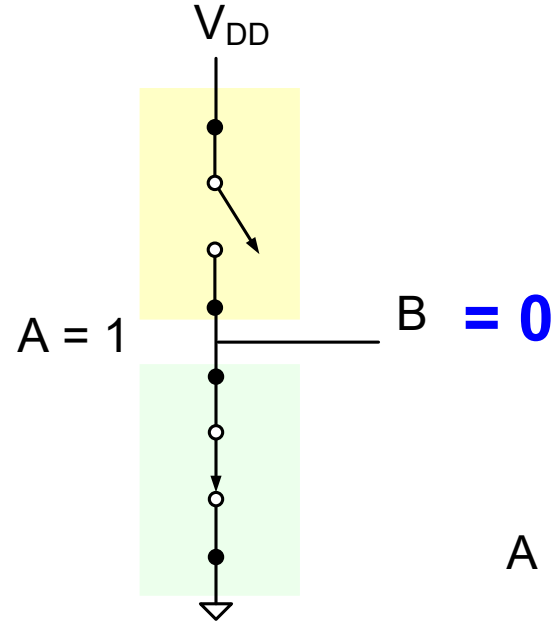
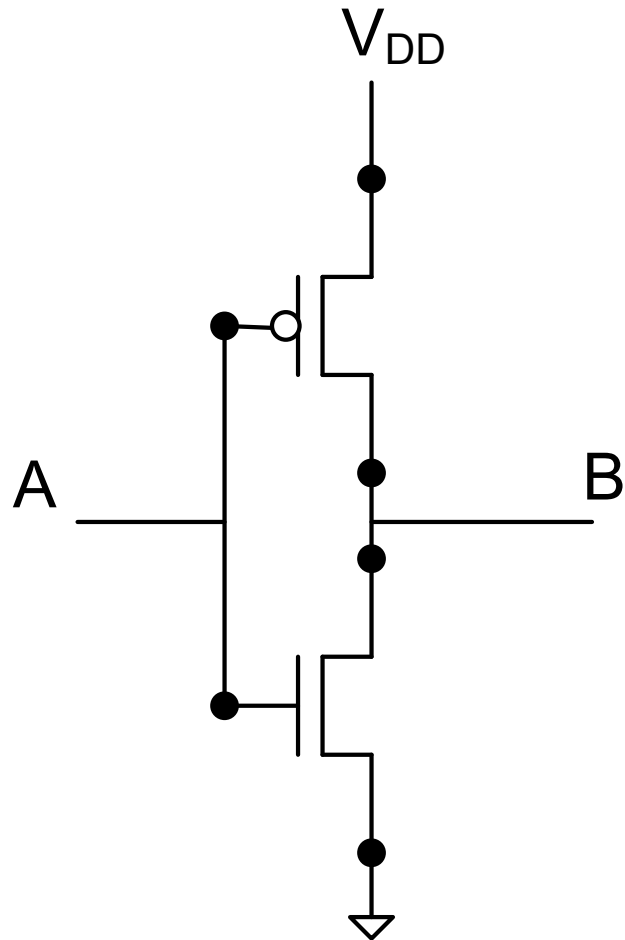
Mathematical model (not dependent upon Boolean notation):

$I_D = 0$ if $|V_{GSp}|$ is small or V_{GSp} is positive

$V_{DS} = 0$ if $|V_{GSp}|$ is large

Review from Last Time

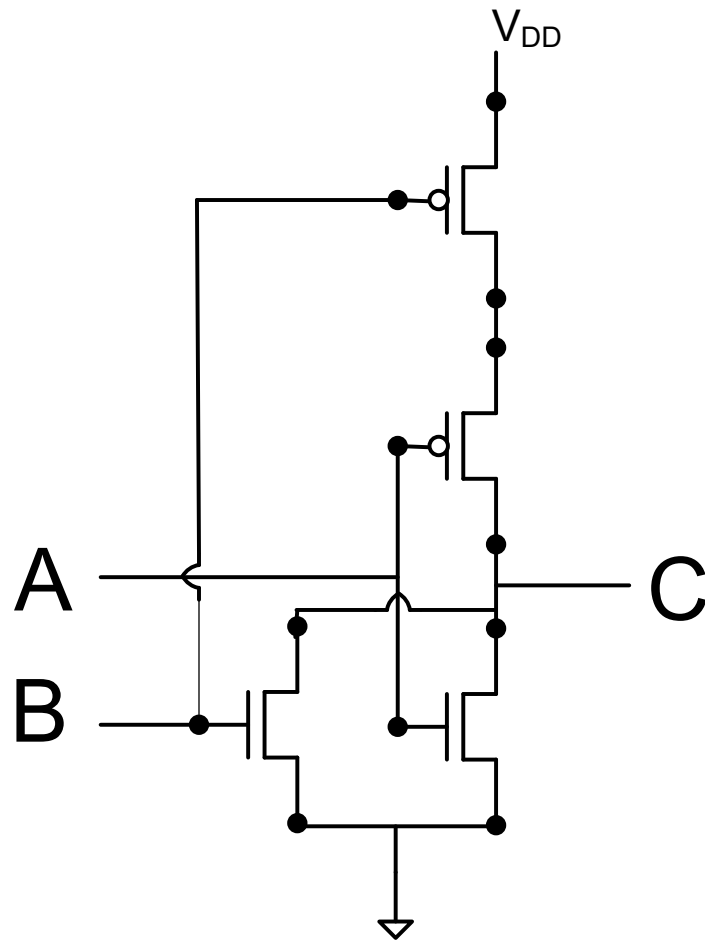
Logic Circuits



Circuit Behaves as a Boolean Inverter

Review from Last Time

Logic Circuits



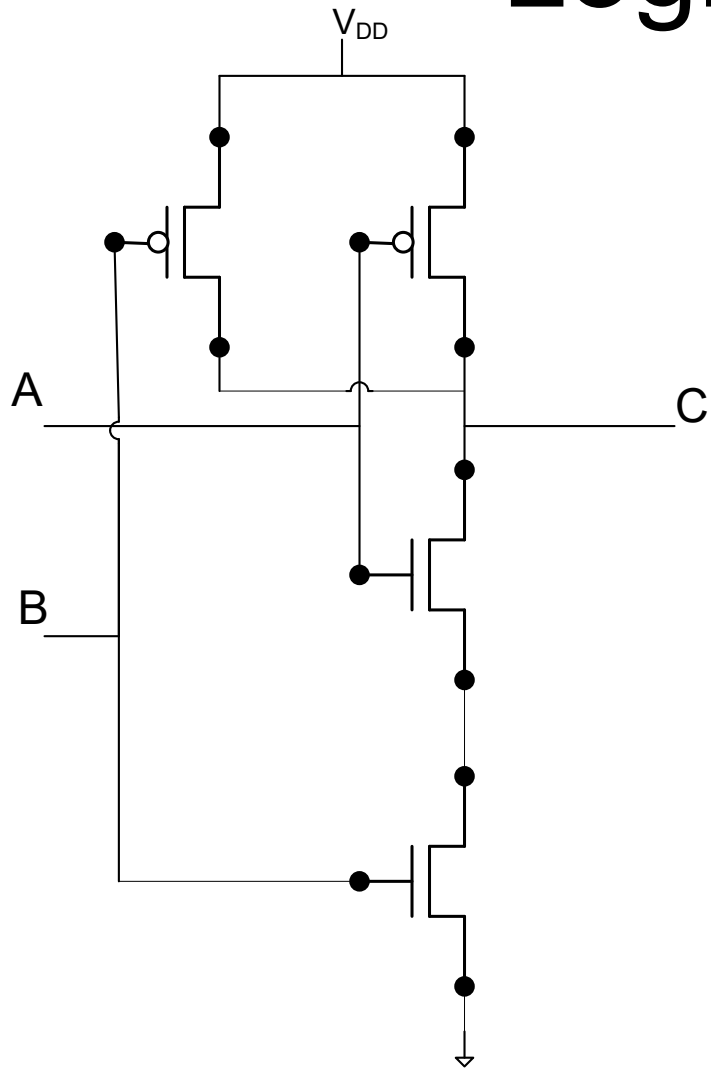
NOR Gate

Truth Table

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Review from Last Time

Logic Circuits



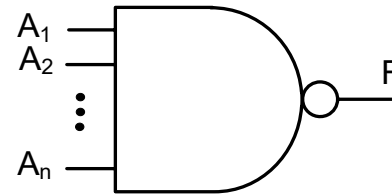
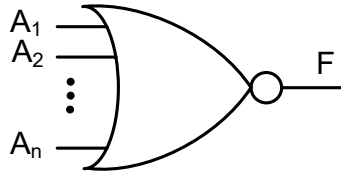
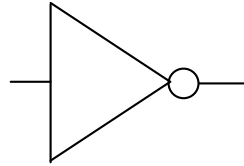
NAND Gate

Truth Table

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

Review from Last Time

Complete Logic Family



Family of n-input NOR gates forms a complete logic family

Family of n-input NAND gates forms a complete logic family

Having both NAND and NOR gates available is a luxury

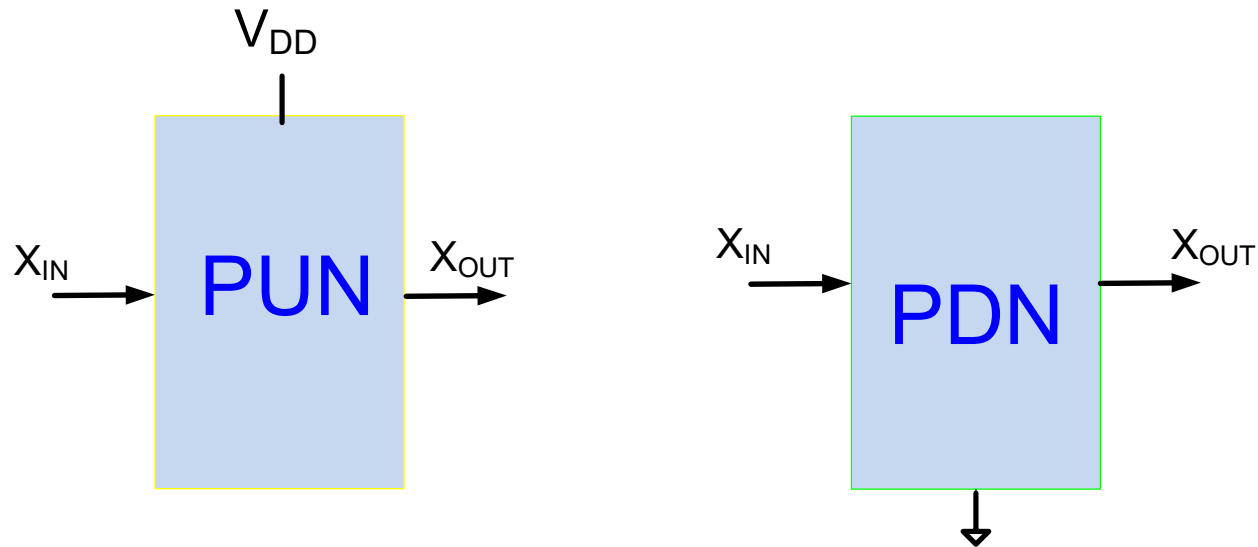
Can now implement any combinational logic function !!

If add one flip flop, can implement any Boolean system !!

Flip flops easy to design but will discuss sequential logic systems later

Review from Last Time

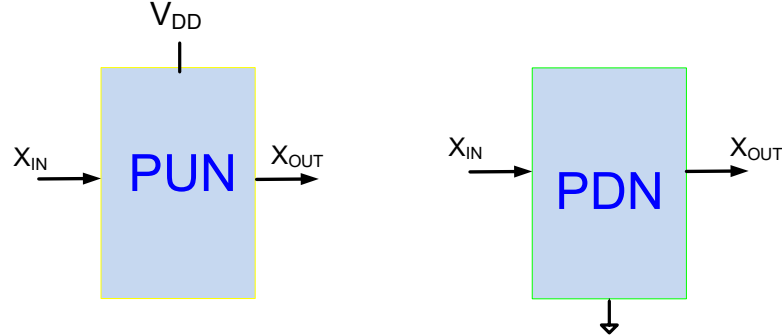
Pull-up and Pull-down Networks



- Pull-Up Network “pulls” output up to V_{DD} in response to some input X_{IN}
- Pull-Down Network “pulls” output down to ground in response to some input X_{IN}

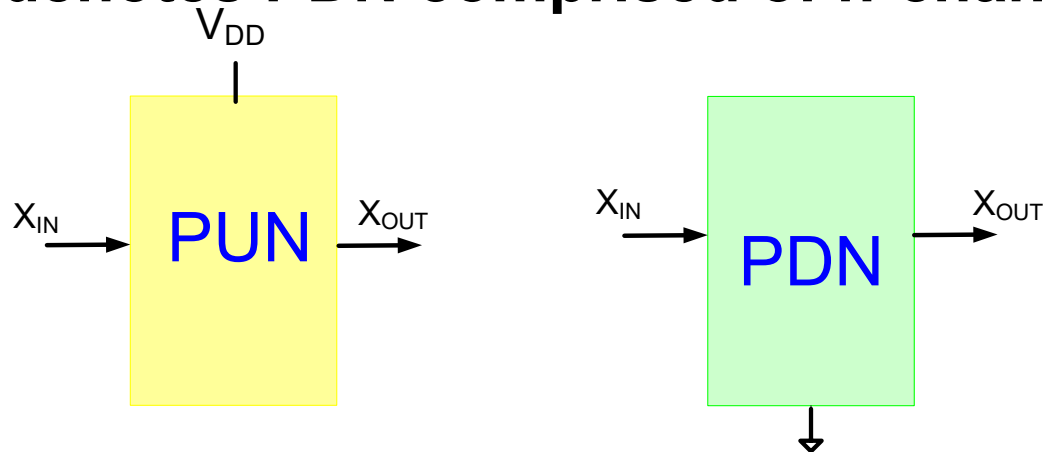
Review from Last Time

Pull-up and Pull-down Networks



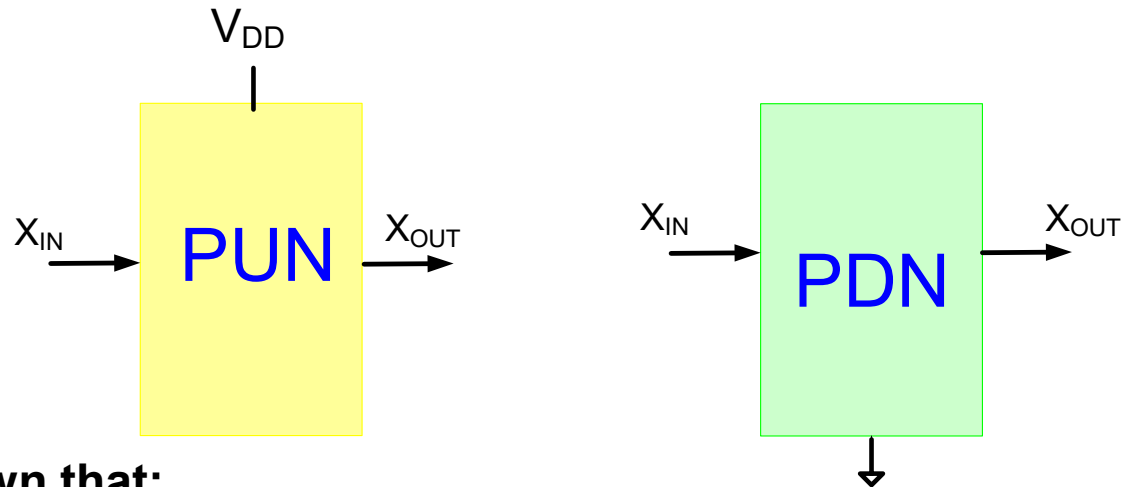
Color convention in following slides (and through much of course)

- **Yellow denotes PUN comprised of p-channel devices**
- **Green denotes PDN comprised of n-channel devices**



Review from Last Time

Pull-up and Pull-down Networks

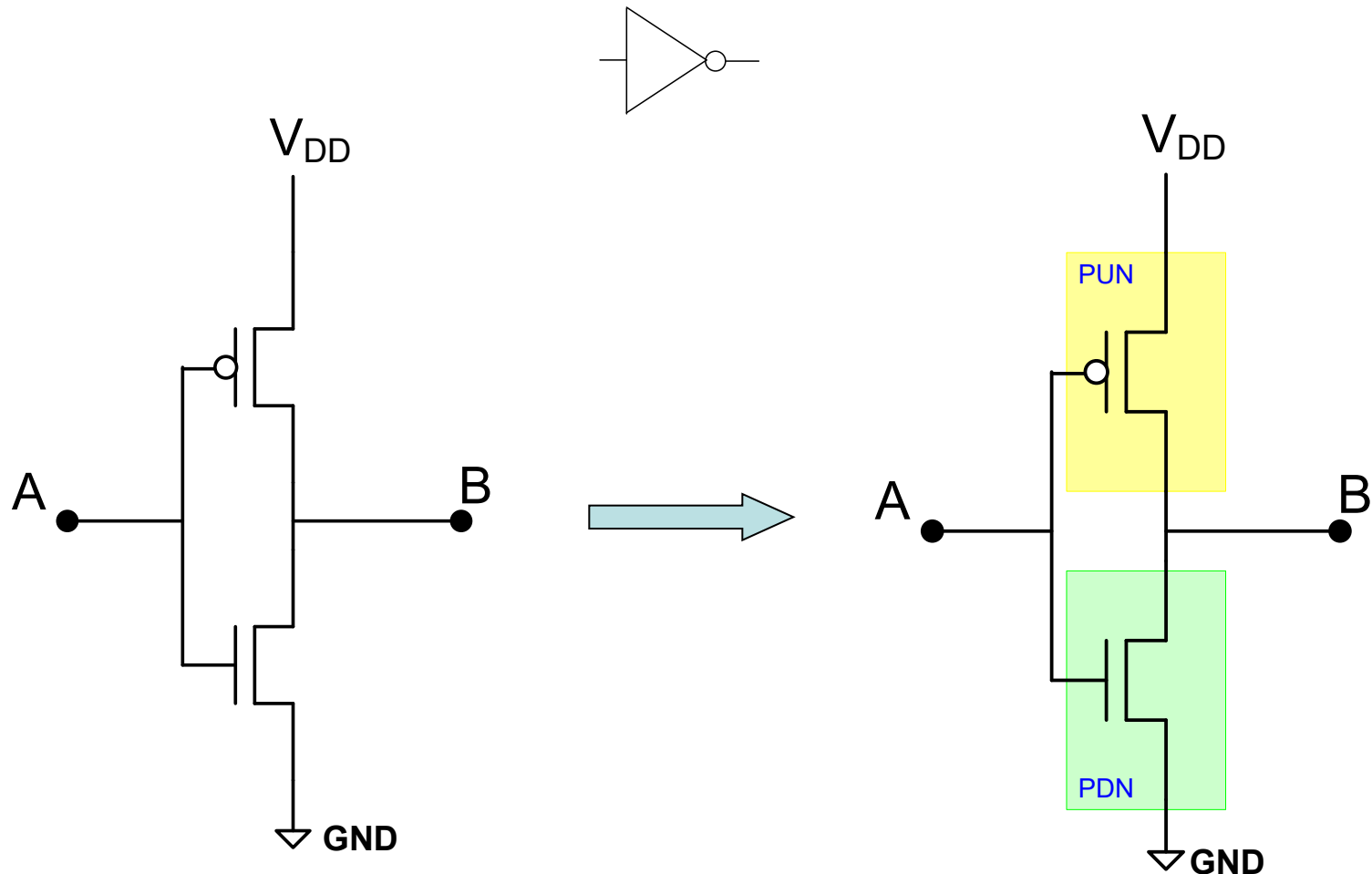


It will be shown that:

- Conduction is via electrons in n-channel devices and via holes in p-channel devices
- Logic circuits comprised entirely of p-channel PUNs and n-channel PDNs have some very attractive electrical properties

Review from Last Time

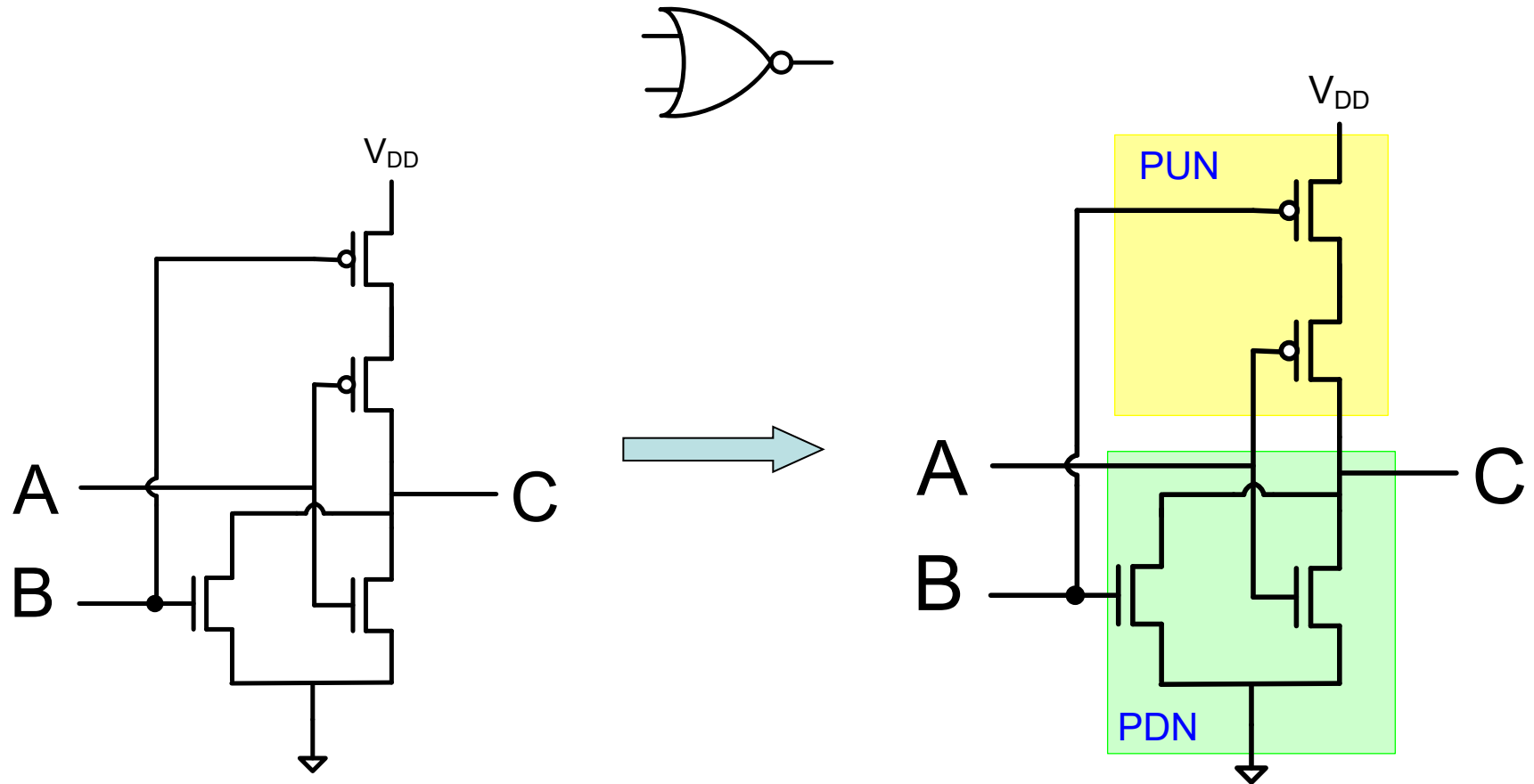
Pull-up and Pull-down Networks



PU network comprised of p-channel device and “tries” to pull B to V_{DD} when conducting
PD network comprised of n-channel device and “tries to pull B to GND when conducting
One and only one of these networks is conducting at the same time (to avoid contention)

Review from Last Time

Pull-up and Pull-down Networks



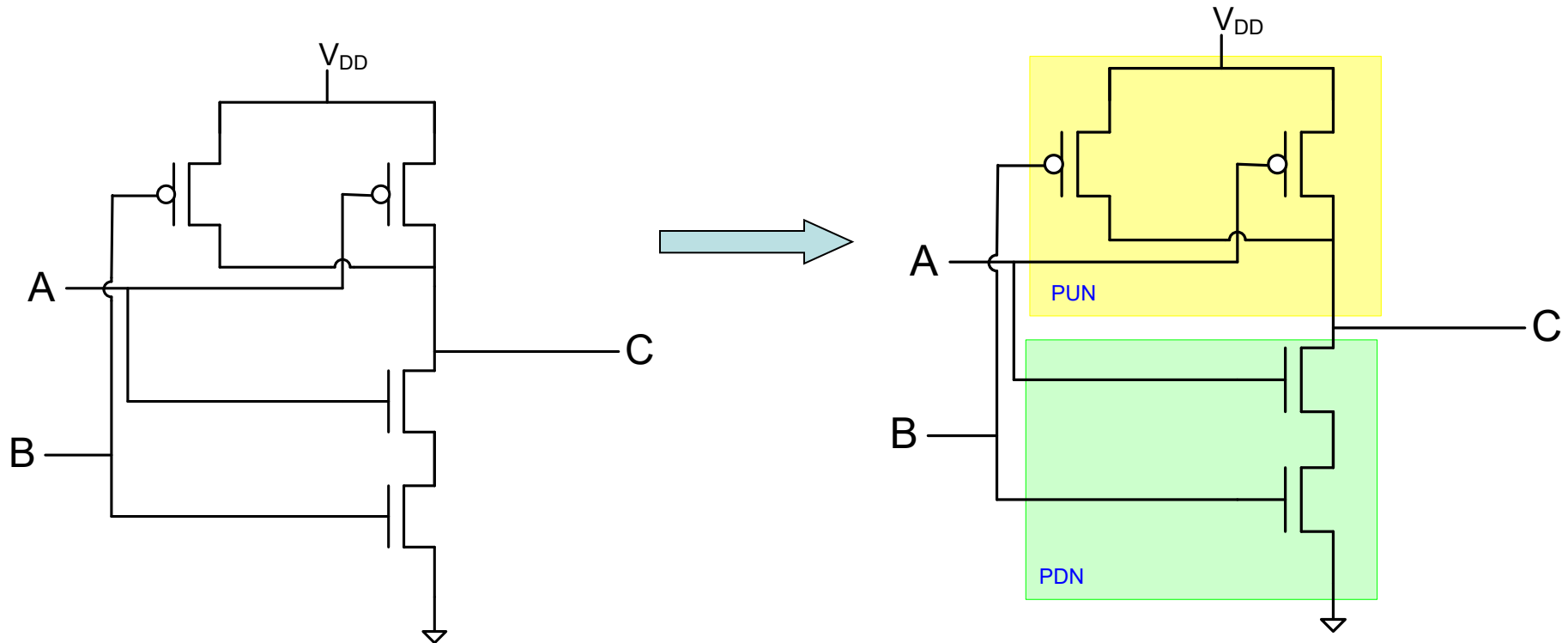
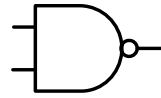
PU network comprised of p-channel devices

PD network comprised of n-channel devices

One and only one of these networks is conducting at the same time

Review from Last Time

Pull-up and Pull-down Networks



PU network comprised of p-channel devices

PD network comprised of n-channel devices

One and only one of these networks is conducting at the same time

Pull-up and Pull-down Networks

Review from Last Time

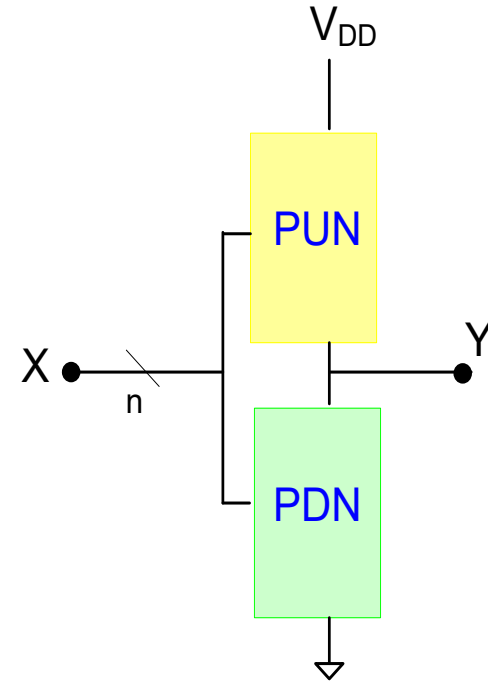
Three key characteristics of Static CMOS Gates

1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time

Three properties of Static CMOS Gates

(based upon simple switch-level model)

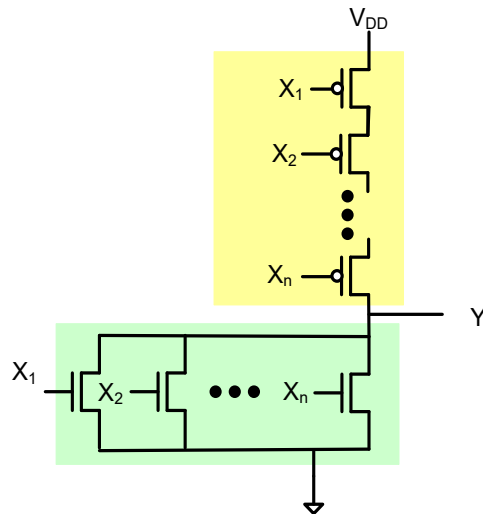
1. $V_H = V_{DD}$, $V_L = 0$ (too good to be true?)
2. $P_H = P_L = 0$ (too good to be true?)
3. $t_{HL} = t_{LH} = 0$ (too good to be true?)



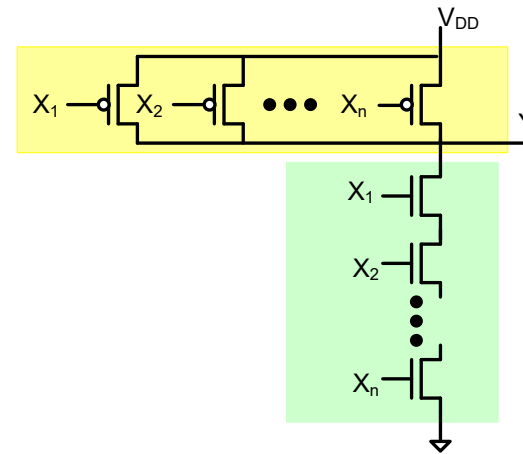
These 3 properties inherent in all Boolean circuits with these 3 characteristics
(provided the ideal switch-level model is used for the transistors)

Review from Last Time

Nomenclature



n-input NOR gate



n-input NAND gate

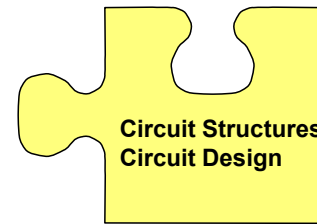
In this class, logic circuits that are implemented by interconnecting multiple-input NAND and NOR gates will be referred to as “Static CMOS Logic”

Since the set of NAND gates is complete, any combinational logic function can be realized with the NAND circuit structures considered thus far

Since the set NOR gates is complete, any combinational logic function can be realized with the NOR circuit structures considered thus far

Many logic functions are realized with “Static CMOS Logic” and this is probably the dominant design style used today!

Example 1:



How many transistors are required to realize the function

$$F = \overline{A} \bullet \overline{B} + \overline{A} \bullet C$$

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

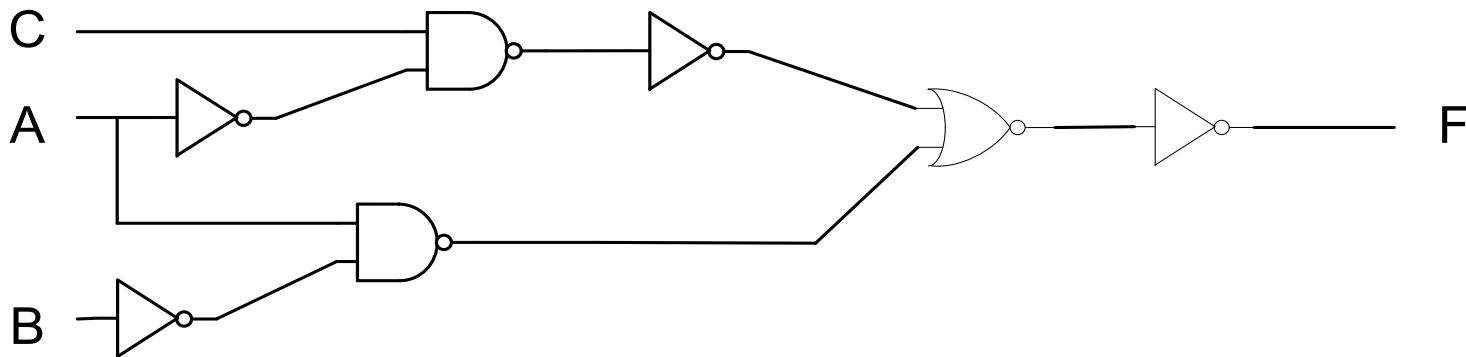
Example 1:

How many transistors are required to realize the function

$$F = \overline{A} \bullet \overline{B} + \overline{A} \bullet C$$

in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Solution:



20 transistors and 5 levels of logic

Example 1:

How many transistors are required to realize the function

$$F = \overline{A} \bullet \overline{B} + \overline{A} \bullet C$$

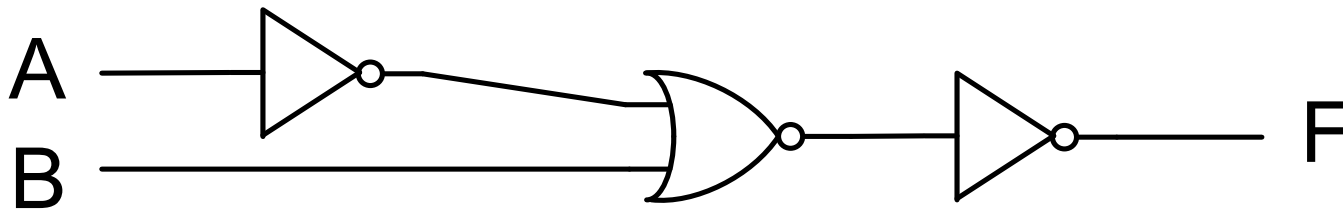
in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Solution (alternative):

From basic Boolean Manipulations

$$F = \overline{A} + \overline{\overline{B}} + \overline{A} \bullet C = \overline{A} + B + \overline{A} \bullet C$$

$$F = \overline{A} \bullet (1 + C) + B = \overline{A} + B$$



8 transistors and 3 levels of logic

Example 1:

How many transistors are required to realize the function

$$F = \overline{A} \bullet \overline{B} + \overline{A} \bullet C$$

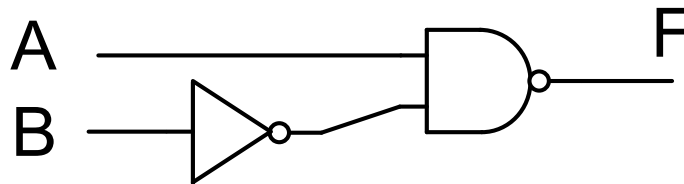
in a basic CMOS process if static NAND and NOR gates are used? Assume A, B and C are available.

Solution (alternative):

From basic Boolean Manipulations

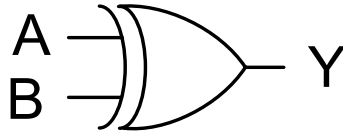
$$F = \overline{A} \bullet (1 + C) + B = \overline{A} + B$$

$$F = \overline{\overline{\overline{A} + B}} = \overline{A \bullet \overline{B}}$$



6 transistors and 2 levels of logic

Example 2: XOR Function

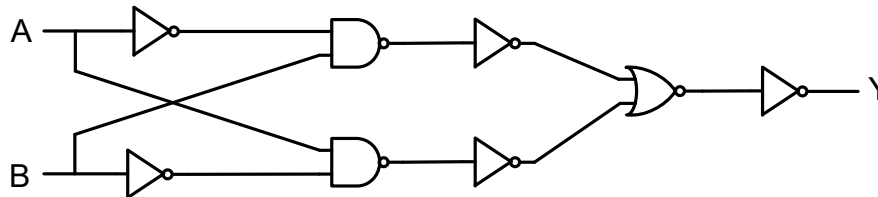


$$Y = A \oplus B$$

A widely-used 2-input Gate

Static CMOS implementation

$$Y = A\bar{B} + \bar{A}B$$

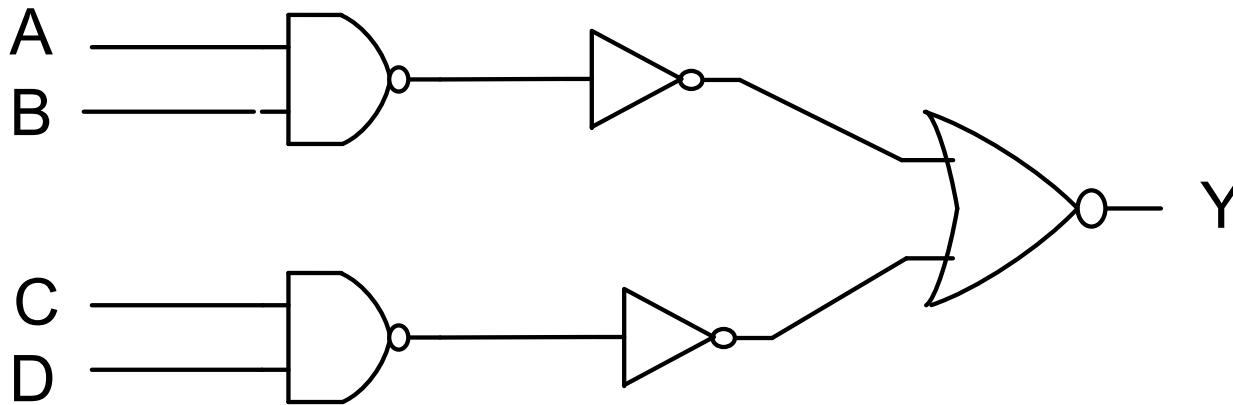


22 transistors 5 levels of logic

Delays unacceptable (will show later) and device count is too large !

Example 3: $Y = \overline{(A \bullet B) + (C \bullet D)}$

Standard Static CMOS Implementation



3 levels of Logic

16 Transistors if Basic CMOS Gates are Used

Can the same Boolean functionality be obtained with less transistors?

Complex Logic Gates

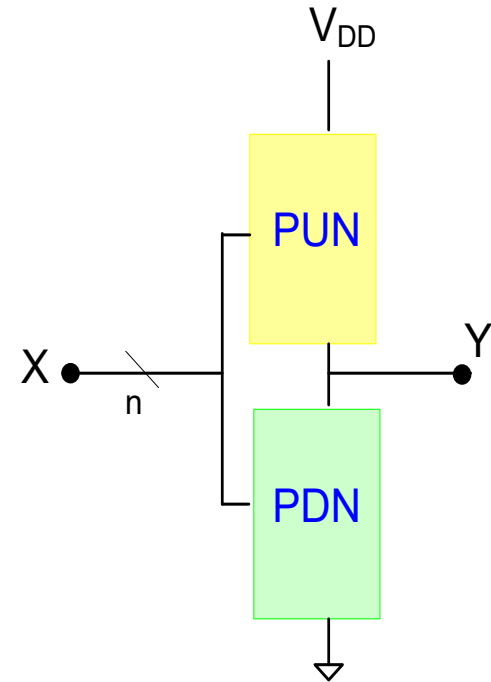
Some circuits other than multiple-input NAND and NOR gates can also have the three key characteristics

Three key characteristics of low static power CMOS logic

1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time

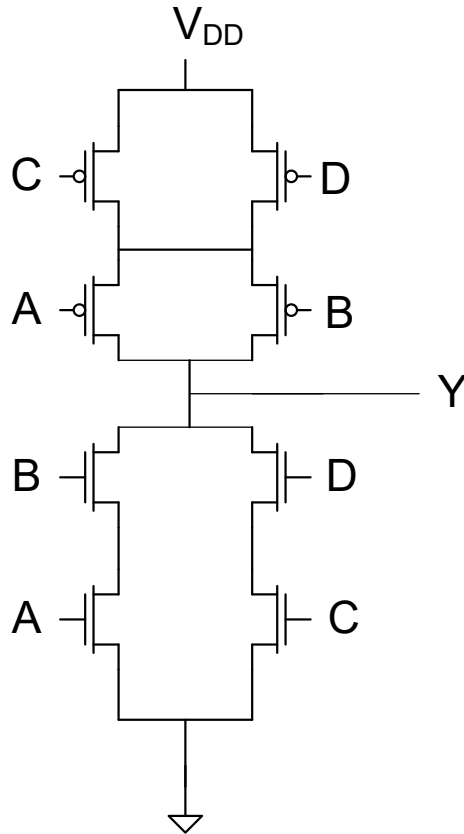
Three properties of circuits with these 3 characteristics

1. $V_H = V_{DD}$, $V_L = 0$ (too good to be true?)
2. $P_H = P_L = 0$ (too good to be true?)
3. $t_{HL} = t_{LH} = 0$ (too good to be true?)

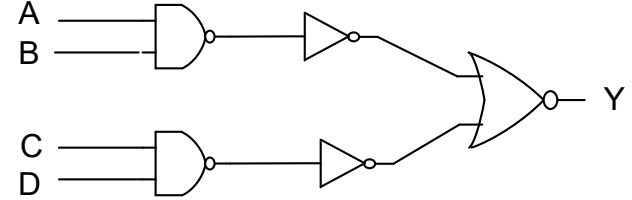


These 3 properties inherent in all Boolean circuits with these 3 characteristics

Observe:



Recall from previous example:



$$Y = \overline{(A \bullet B) + (C \bullet D)}$$

3 levels of Logic, 16 Transistors if Basic CMOS Gates are Used

$$Y = \overline{(A \bullet B) + (C \bullet D)}$$

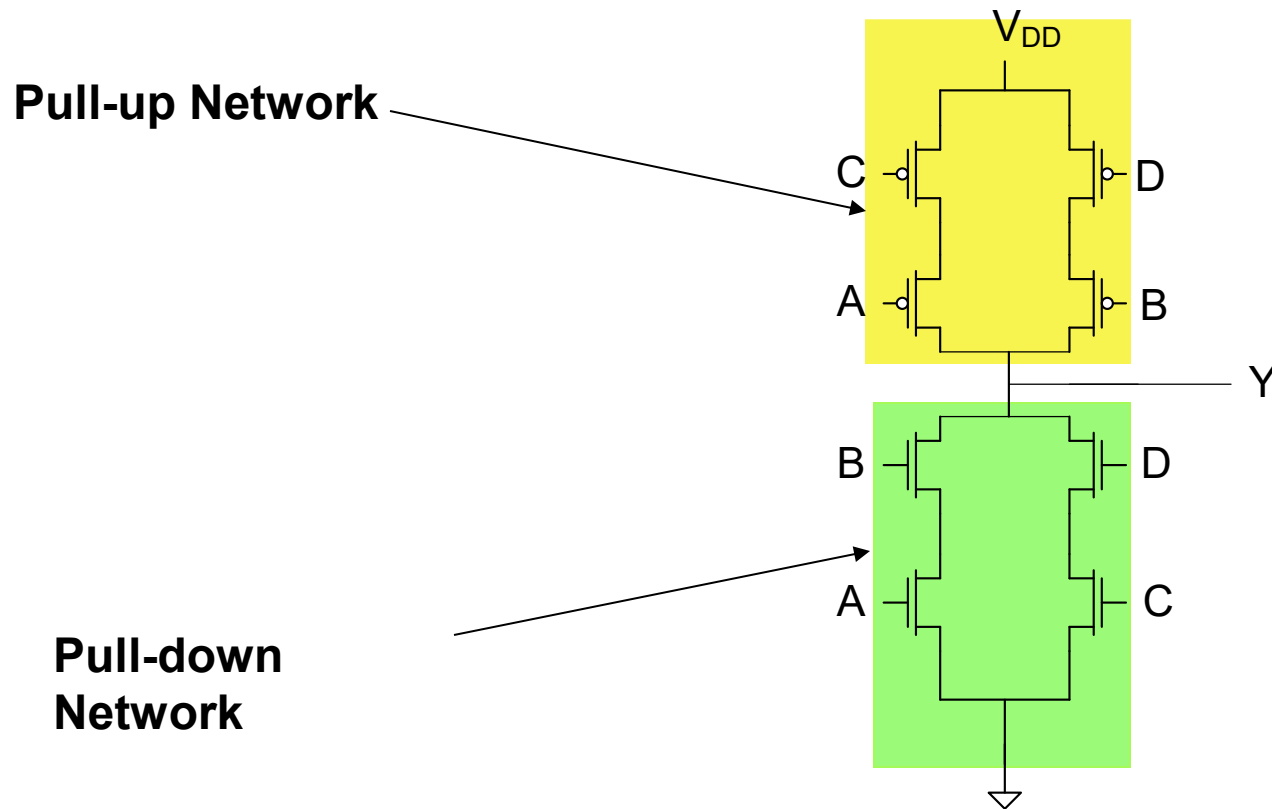
1 level of logic and 8 transistors in this example

Significant reduction in transistor count and levels of logic for realizing same Boolean function

Termed a “Complex Logic Gate” implementation

Some authors term this a “compound gate”

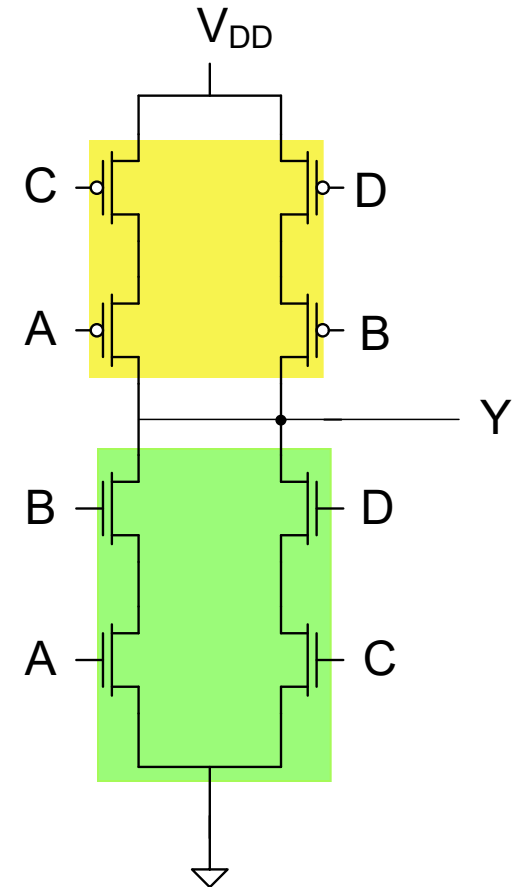
Complex Logic Gates



$$Y = \overline{(A \bullet B) + (C \bullet D)}$$

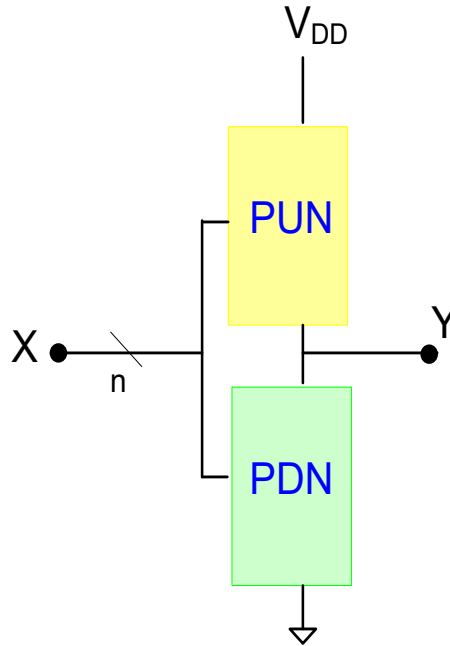
Complex Gates

1. PU network comprised of p-channel devices
2. PD network comprised of n-channel devices
3. One and only one of these networks is conducting at the same time
4. Boolean Function Realized from Inputs (or complimented inputs) in one level of logic



Complex Gates

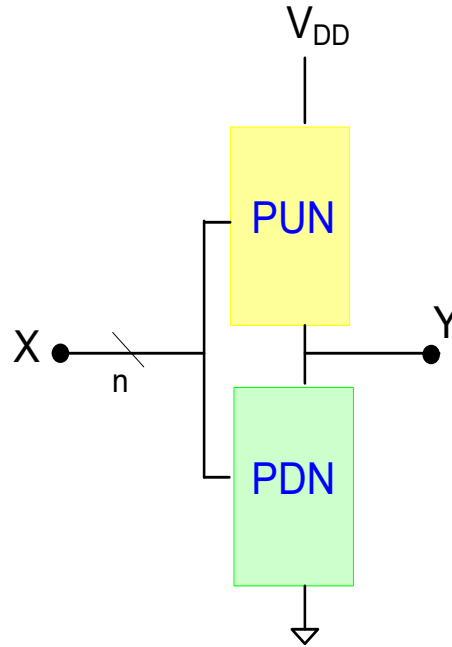
Nomenclature:



When the logic gate shown is not a multiple-input NAND or NOR gate but has Characteristics 1, 2, 3, and 4 above, the gate will be referred to as a Complex Logic Gate

Complex Logic Gates also implement static logic functions and some authors would refer to this as Static CMOS Logic as well but we will make the distinction and refer to this as “Complex Logic Gates”

Complex Gates

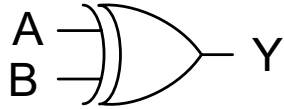


Complex Gate Design Strategy:

1. Implement $\bar{Y}$ in the PDN
2. Implement Y in the PUN (must complement the input variables since p-channel devices are used)

(Y and $\bar{Y}$ often expressed in either SOP or POS form)

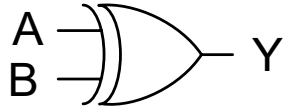
XOR in Complex Logic Gates



$$Y = A \oplus B$$

Will express $\overline{Y}$ and Y in standard SOP or POS form

XOR in Complex Logic Gates



$$Y = A \oplus B$$

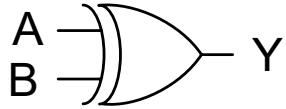
$$Y = A\bar{B} + \bar{A}B$$

$$\bar{Y} = \overline{(A\bar{B} + \bar{A}B)}$$

$$\bar{Y} = \overline{A\bar{B}} \bullet \overline{\bar{A}B}$$

$$\bar{Y} = (\bar{A} + B) \bullet (A + \bar{B})$$

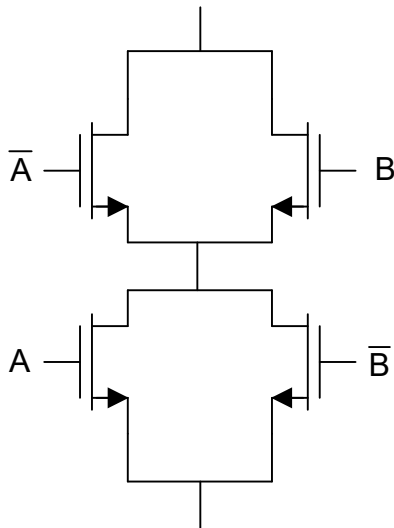
XOR in Complex Logic Gates



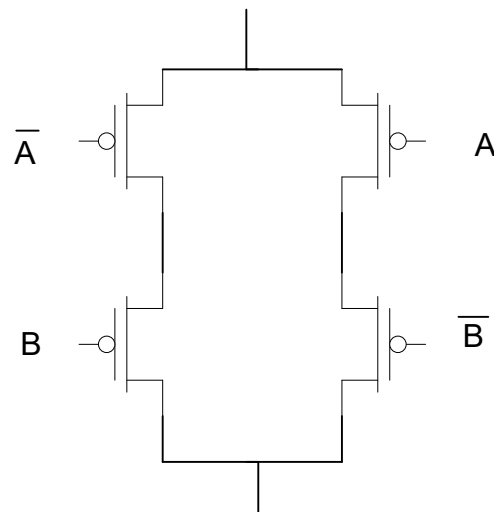
$$Y = A\bar{B} + \bar{A}B$$

$$\bar{Y} = (\bar{A} + B) \cdot (A + \bar{B})$$

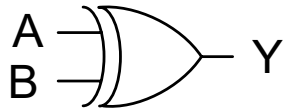
PDN



PUN

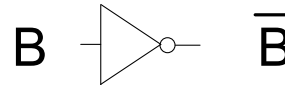
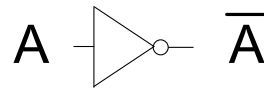


XOR in Complex Logic Gates



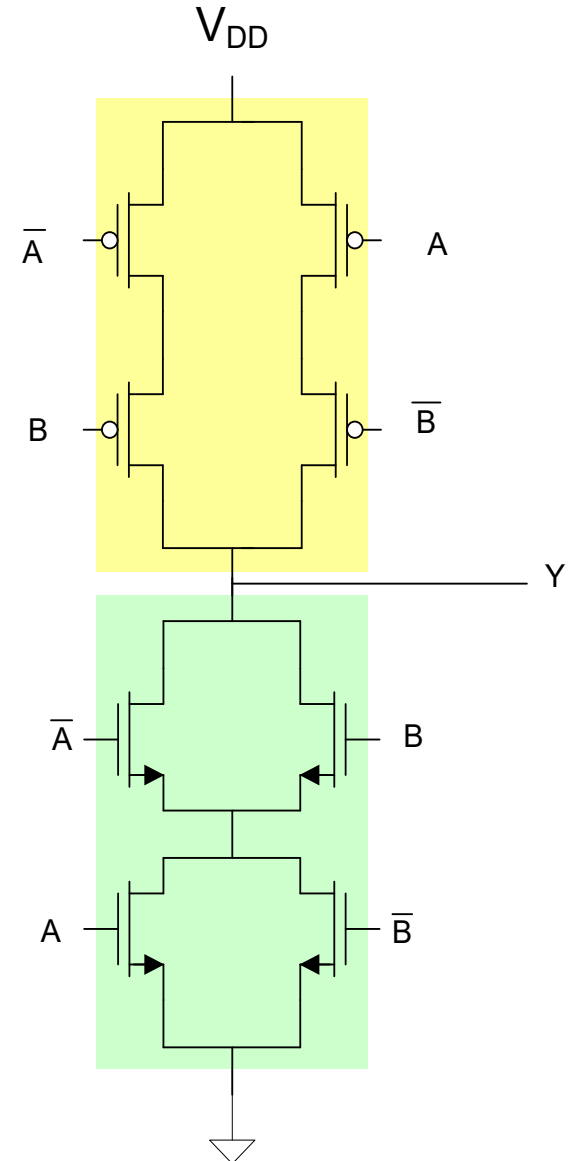
$$Y = A\bar{B} + \bar{A}B$$

$$\bar{Y} = (\bar{A} + B) \cdot (A + \bar{B})$$

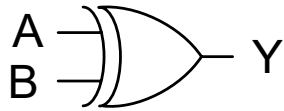


12 transistors and 2 levels of logic

Notice a significant reduction in the number of transistors required

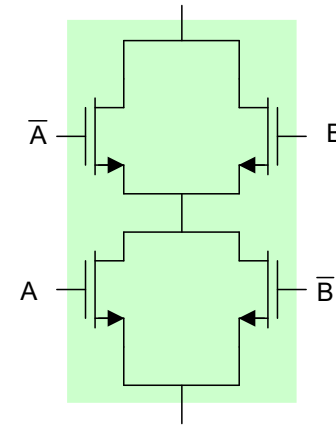


XOR in Complex Logic Gates



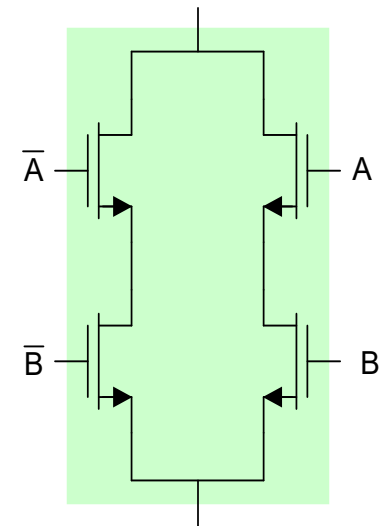
$$Y = A\bar{B} + \bar{A}B$$

$$\bar{Y} = (\bar{A} + B) \cdot (A + \bar{B})$$

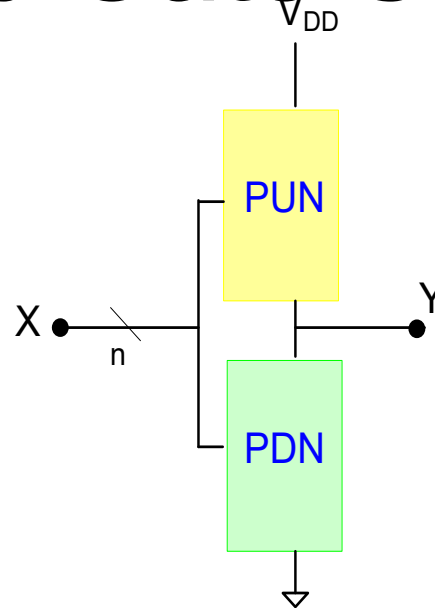


Multiple PU and PD networks can be used

$$\begin{aligned}\bar{Y} &= (\bar{A} + B) \cdot (A + \bar{B}) \\ &= (\bar{A} \cdot (A + \bar{B})) + (B \cdot (A + \bar{B})) \\ &= (\bar{A} \cdot \bar{B}) + (A \cdot B)\end{aligned}$$



Complex Logic Gate Summary:



If PUN and PDN satisfy the characteristics:

1. PU network comprised of p-channel device
2. PD network comprised of n-channel device
3. One and only one of these networks is conducting at the same time

Properties of PU/PD logic of this type (with simple switch-level model):

Rail to rail logic swings

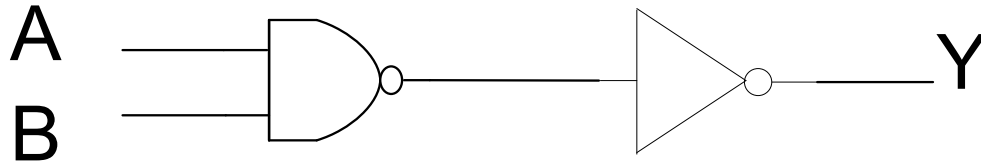
Zero static power dissipation in both $Y=1$ and $Y=0$ states

Arbitrarily fast (too good to be true? will consider again with better model)

Pass Transistor Logic

Consider $Y = A \bullet B$

Standard CMOS Implementation

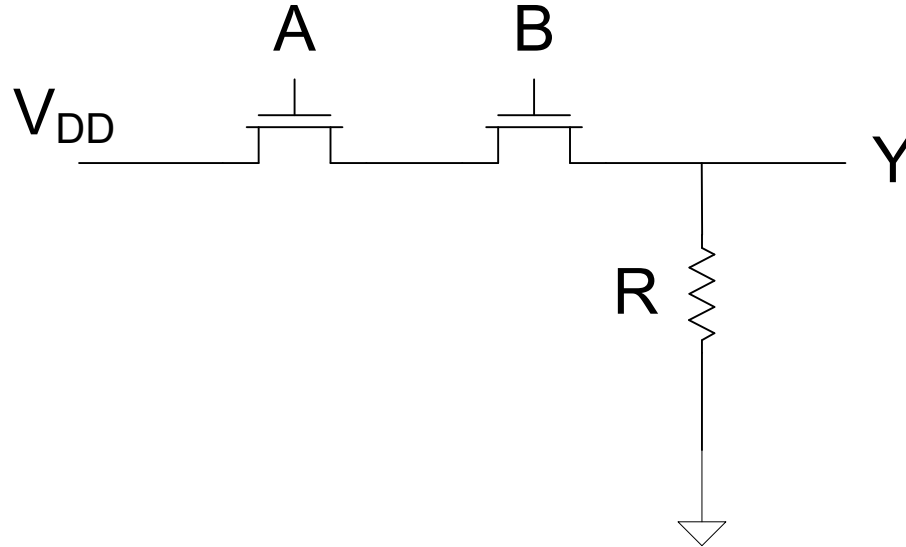


2 levels of Logic

6 Transistors if Basic CMOS Gates are Used

Basic noninverting functions generally require more complexity if basic CMOS gates are used for implementation

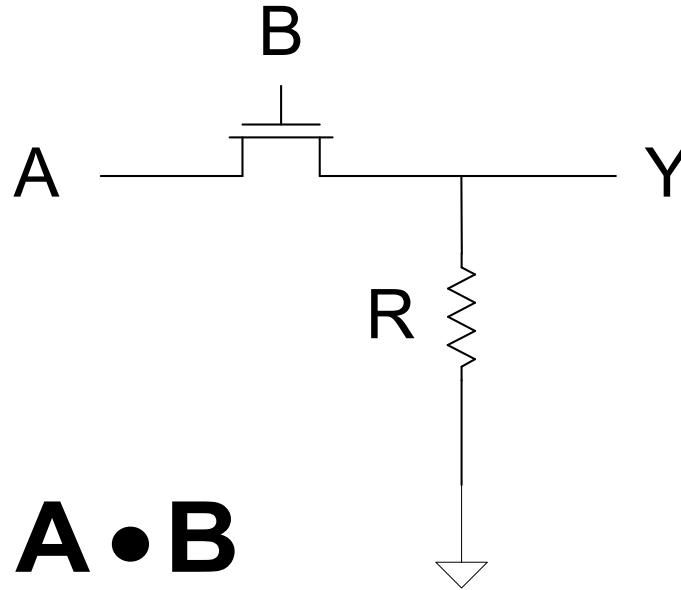
Pass Transistor Logic



$$Y = A \bullet B$$

Requires only 2 transistors rather than 6 for a standard CMOS gate (and a resistor).

Pass Transistor Logic



$$Y = A \bullet B$$

Even simpler pass transistor logic implementations are possible

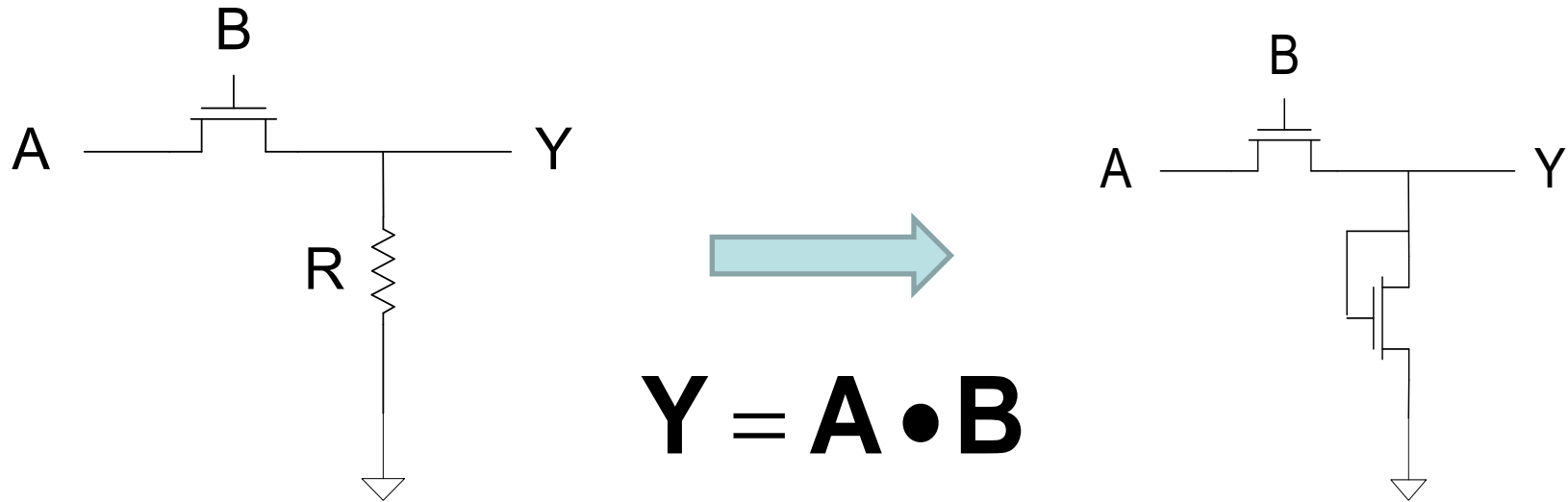
Requires only 1 transistor (and a resistor).



Will see later that the area of a single practical resistor for this circuit may be comparable to that needed for hundreds or even thousands of transistors



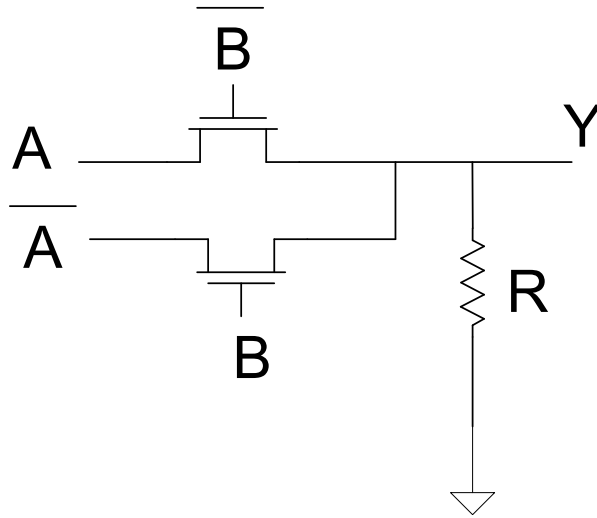
Pass Transistor Logic



- May be able to replace resistor with transistor (one of several ways shown)
- But high logic level can not be determined with existing device model (or even low logic level for circuit on right)
- Power dissipation can not be determined with existing device model for circuit on right

Better device model is needed (Power? Signal Swing? Speed?)

Pass Transistor Logic



$$Y = A \oplus B$$

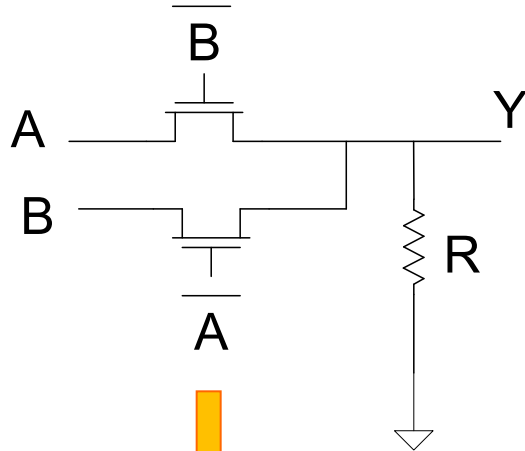


$$Y = A\bar{B} + \bar{A}B$$

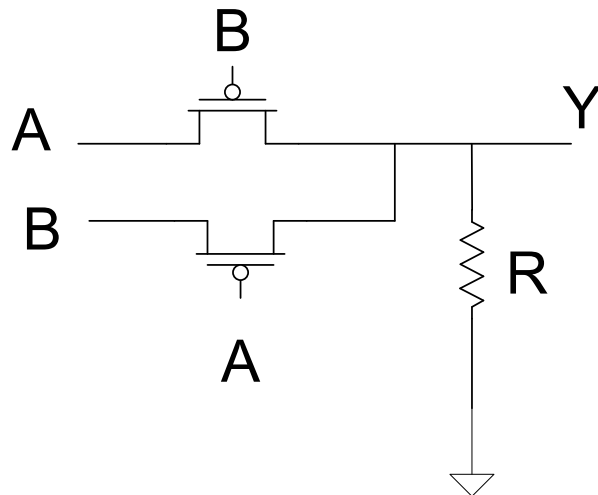
6 transistors, 1 resistor, two levels of logic

(the 4 transistors in the two inverters needed to generate $\bar{A}$ and $\bar{B}$ are not shown)

Pass Transistor Logic



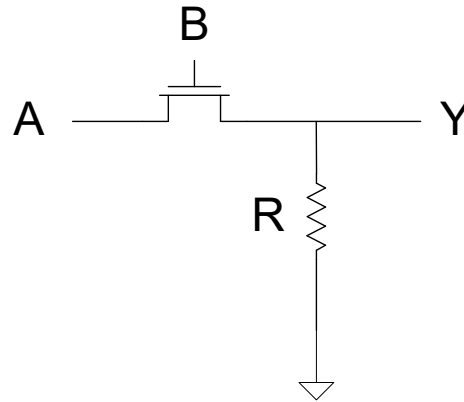
$$Y = A \oplus B$$



$$Y = A \oplus B$$

2 transistors, 1 resistor, one level of logic

Pass Transistor Logic



Requires only 1 transistor (and a resistor)

- Pass transistor logic can offer significant reductions in complexity for some functions (particularly noninverting)
- Resistor may require more area than several hundred or even several thousand transistors
- Signal levels may not go to V_{DD} or to 0V
- Static power dissipation may not be zero
- Signals may degrade unacceptably if multiple gates are cascaded
- “resistor” often implemented with a transistor to reduce area but signal swing and power dissipation problems still persist
- Pass transistor logic is widely used

Logic Design Styles

- Several different logic design styles are often used throughout a given design (3 considered thus far)
 - Static CMOS
 - Complex Logic Gates
 - Pass Transistor Logic
- The designer has complete control over what is placed on silicon and governed only by cost and performance
- New logic design strategies have been proposed recently and others will likely emerge in the future
- The digital designer needs to be familiar with the benefits and limitations of varying logic styles to come up with a good solution for given system requirements

Improved Switch-Level Models

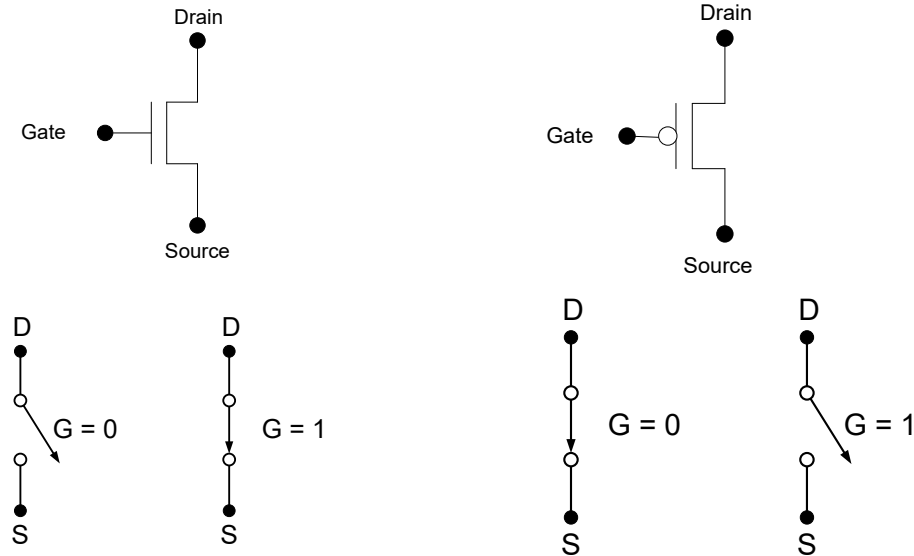
MOSFET Modeling



- Simple model of MOSFET was developed (termed switch-level model)
- Simple gates designed in CMOS Process were introduced
 - Some have zero power dissipation
 - Some have or appeared to have rail to rail logic voltage swings
 - All appeared to be Infinitely fast
 - Logic levels of some can not be predicted with simple model
 - Simple model is not sufficiently accurate to provide insight relating to some of these properties
- MOSFET modeling strategy
 - hierarchical model structure will be developed
 - generally use simplest model that can be justified

MOS Transistor Models

1, Switch-Level model



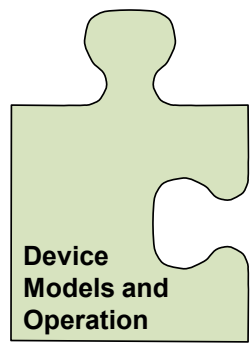
Advantages:

Simple, does not require understanding of semiconductor properties, does not depend upon process, adequate for understanding basic operation of many digital circuits

Limitations:

Does not provide timing information (surfaced when looking at static CMOS circuits, and several others that have not yet become apparent from the applications that have been considered) and can not support design of “resistor” used in Pass Transistor Logic

Improved Device Models



With the simple switch-level model, it was observed that basic static CMOS logic gates have the following three properties:

- Rail to rail logic swings
- Zero static power dissipation in both $Y=1$ and $Y=0$ states
- Arbitrarily fast (too good to be true? will consider again with better model)

It can be shown that the first two properties are nearly satisfied in actual fabricated circuits with p-channel/n-channel PU/PD logic but though the circuits are fast, they are observably not arbitrarily fast

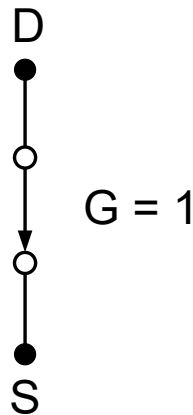
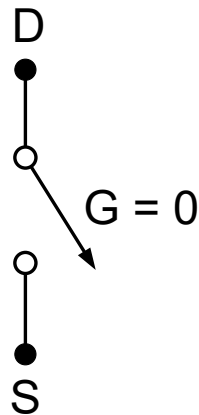
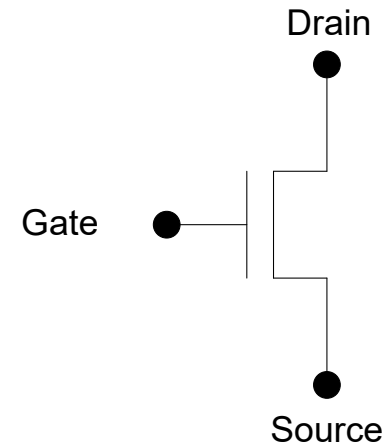
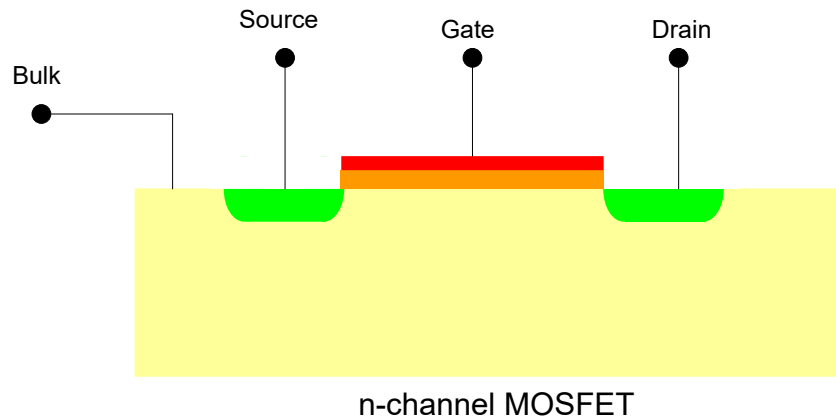
None of these properties are observed for some logic styles such as Pass Transistor Logic

Will now extend switch-level model to predict speed of basic gates in static CMOS and logic levels and power dissipation in PTL

Recall

MOS Transistor

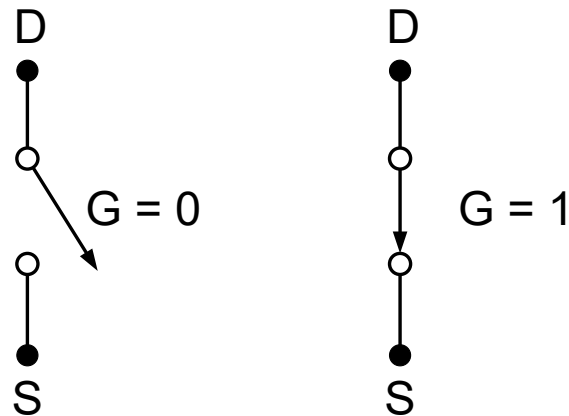
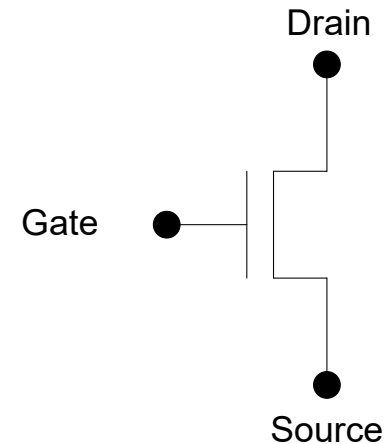
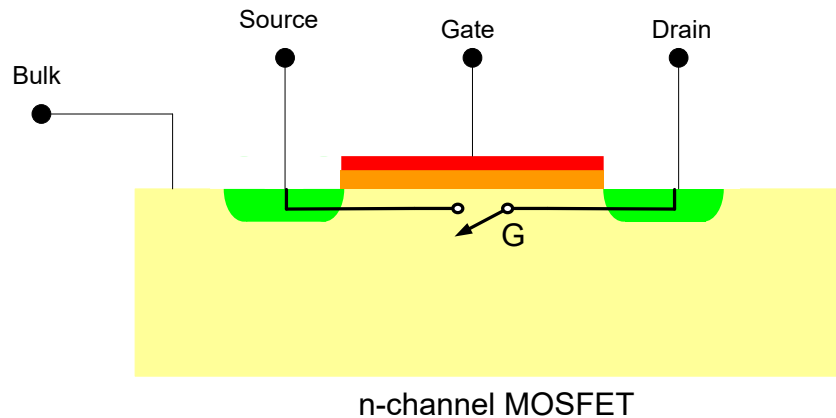
Qualitative Discussion of n-channel Operation



This was the first model introduced and was termed the basic switch-level mode

MOS Transistor

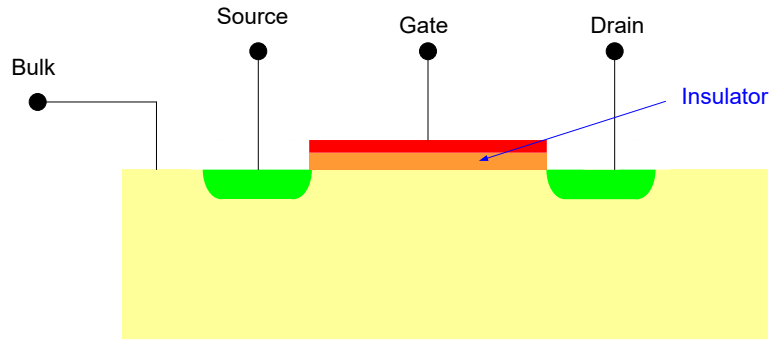
Qualitative Discussion of n-channel Operation



Conceptual view of basic switch-level model

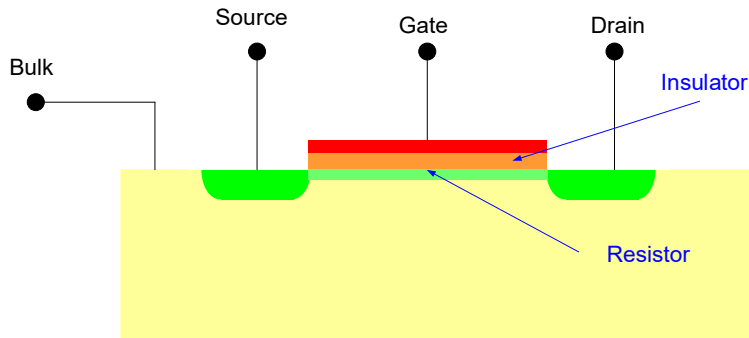
MOS Transistor

Qualitative Discussion of n-channel Operation



n-channel MOSFET

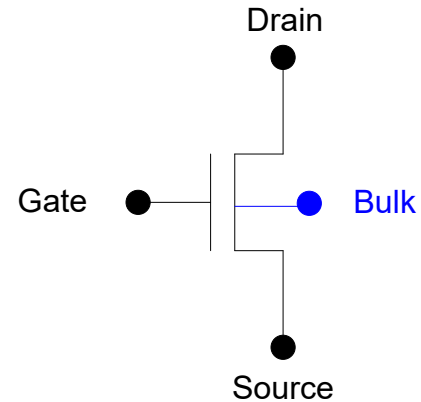
For V_{GS} small



n-channel MOSFET

For V_{GS} large

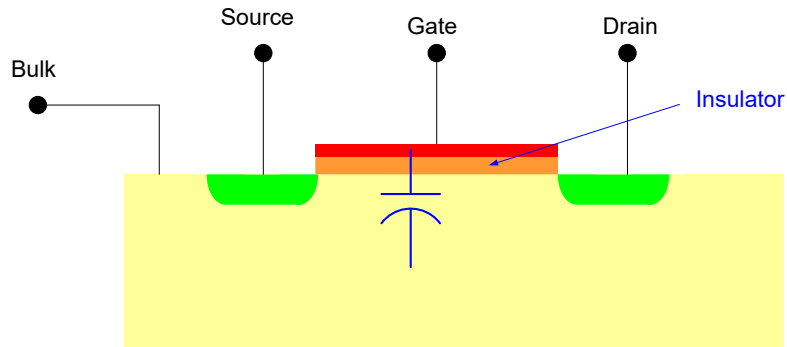
- Region under gate termed the “channel”
- When “resistor” is electrically created, region where it resides in channel is termed an “inversion region”



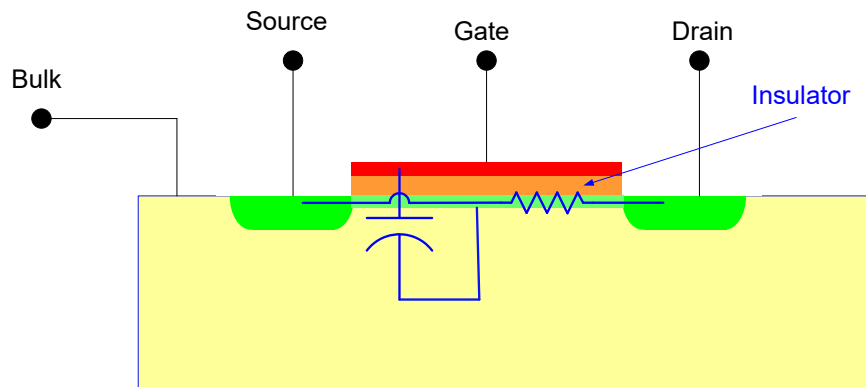
MOSFET actually 4-terminal device

MOS Transistor

Qualitative Discussion of n-channel Operation



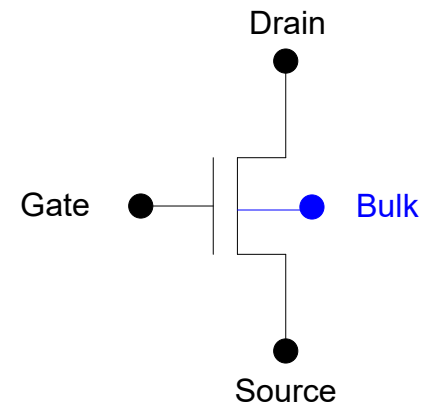
For V_{GS} small



n-channel MOSFET

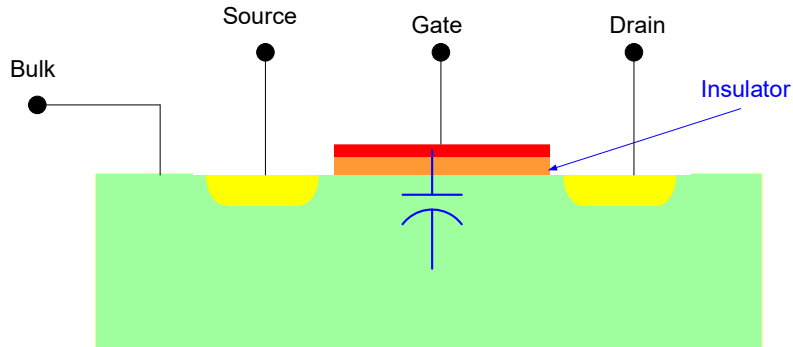
For V_{GS} large

- Electrically created inversion layer forms a “thin “film” resistor
- Capacitance from gate to channel region is distributed
- Lumped capacitance much easier to work with



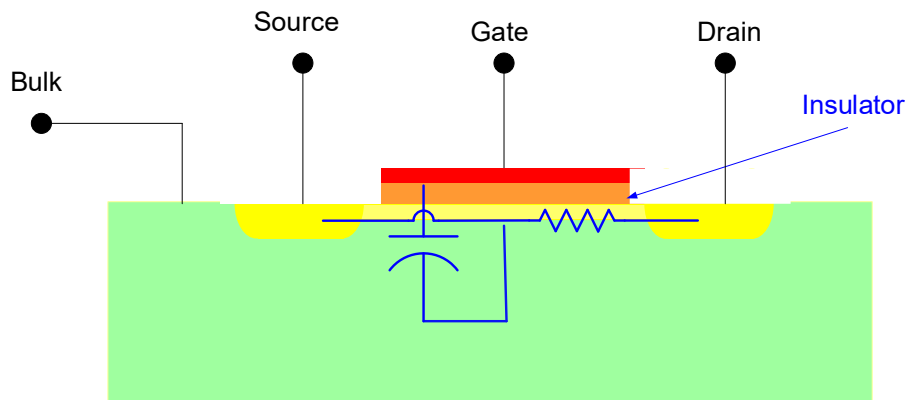
MOS Transistor

Qualitative Discussion of p-channel Operation

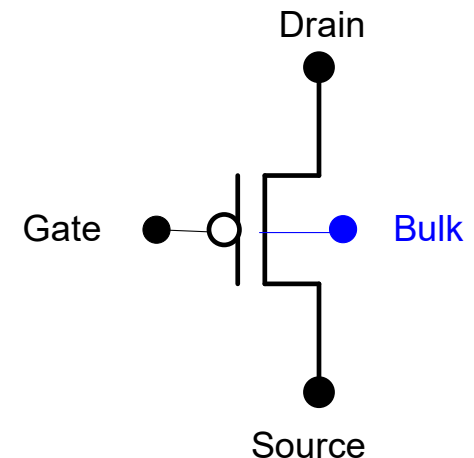


p-channel MOSFET

For $|V_{GS}|$ small



p-channel MOSFET

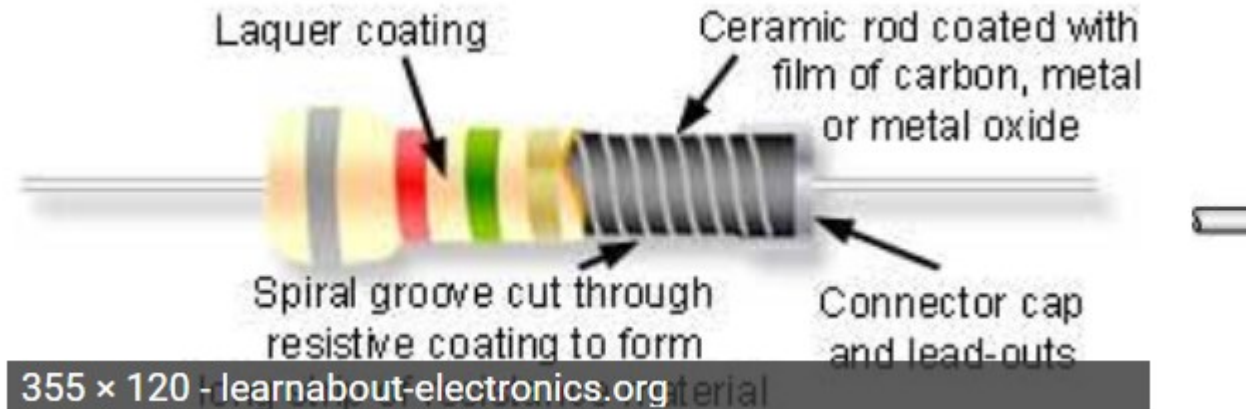


For $|V_{GS}|$ large

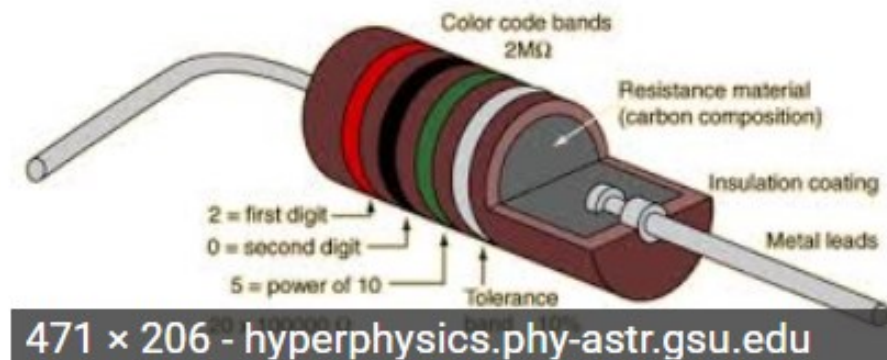
- Electrically created inversion layer forms a “thin “film” resistor
- Capacitance from gate to channel region is distributed
- Lumped capacitance much easier to work with

Discrete Resistors often use thin films too though not electrically created

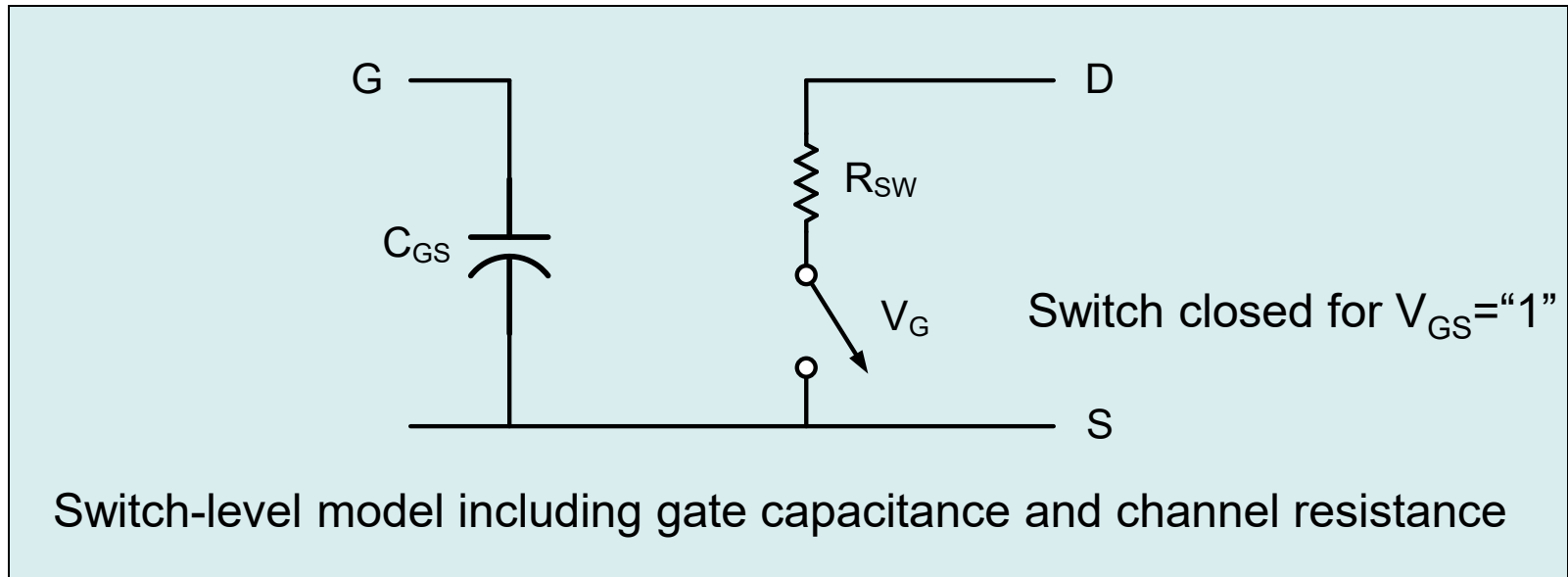
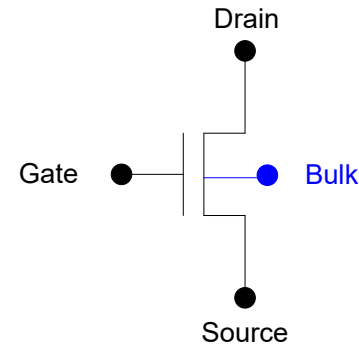
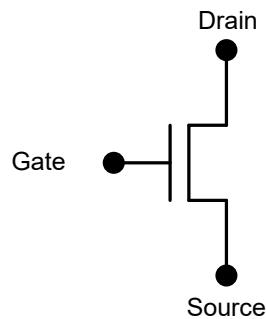
- Thin-film spiral wound



- Carbon composition

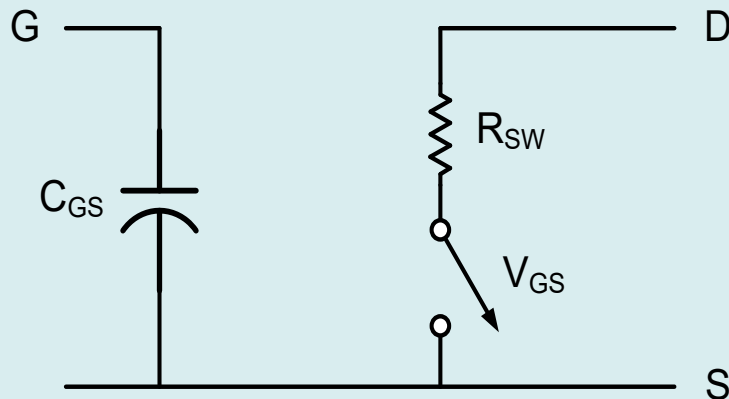
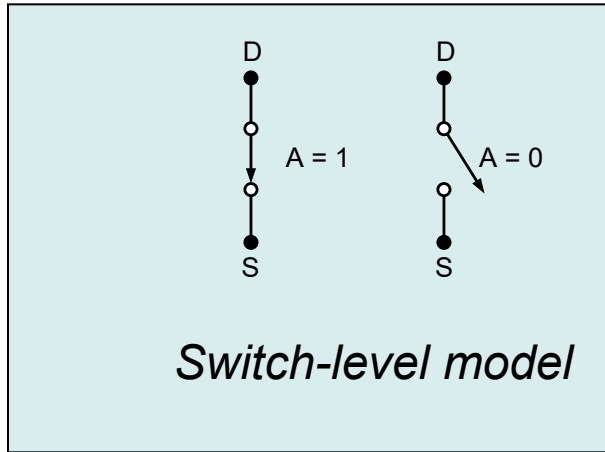
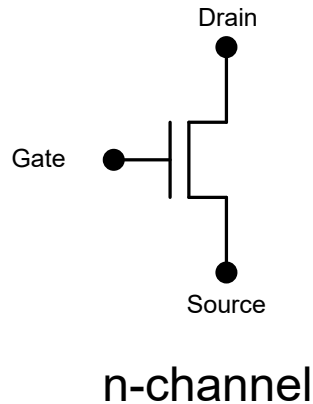


Improved Switch-Level Model



- Connect the gate capacitance to the source to create lumped model
- Still neglect bulk connection

Improved Switch-Level Model



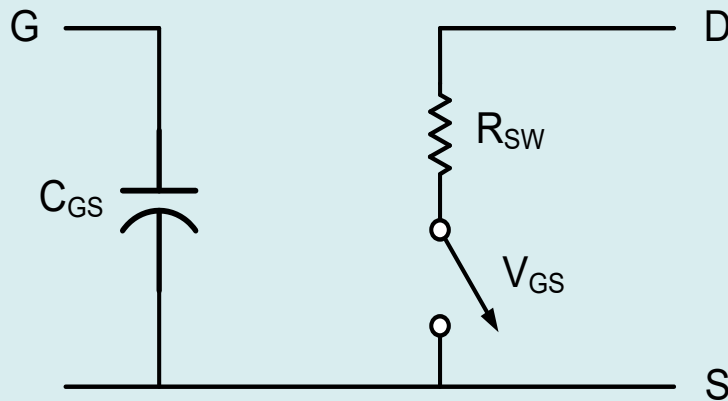
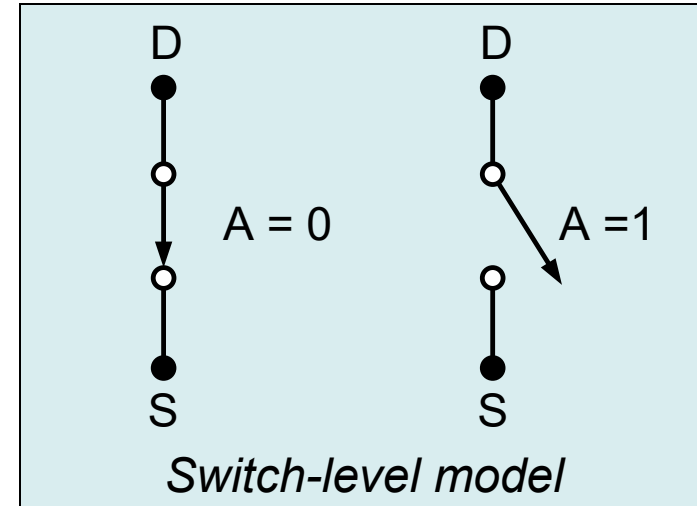
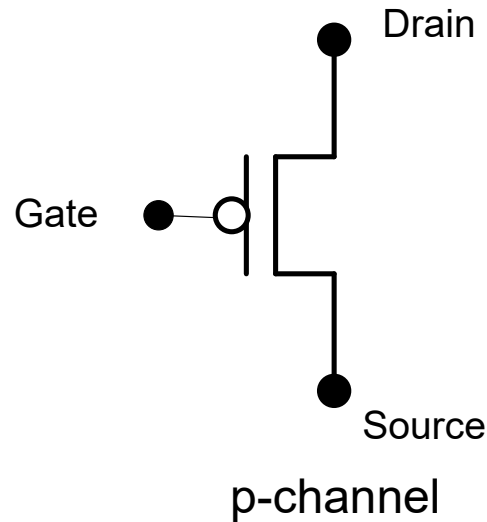
Switch closed for $V_{GS} = \text{large}$

Alt: switch closed for "A = 1"

A denotes Boolean signal on Gate

Switch-level model including gate capacitance and channel resistance

Improved Switch-Level Model



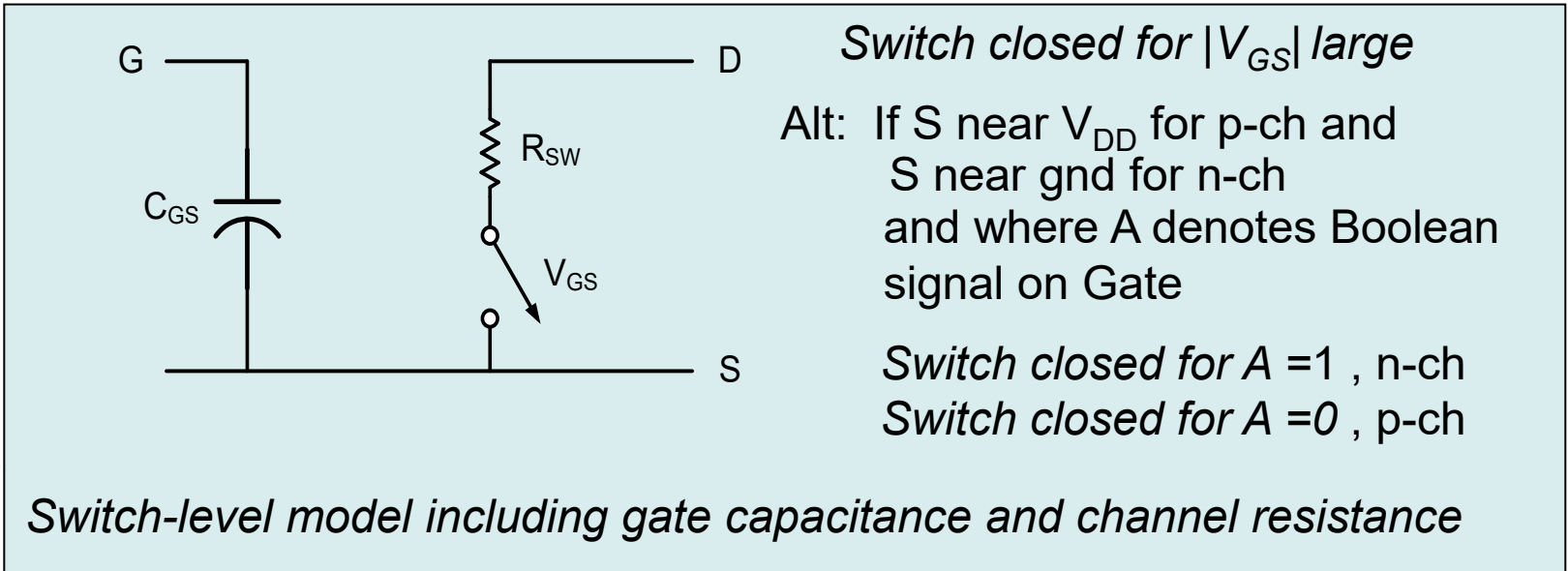
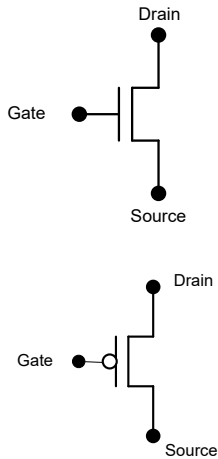
Switch closed for $|V_{GS}|$ large

Alt: If S near V_{DD} , closed for $A=0$

A denotes Boolean signal on Gate

Switch-level model including gate capacitance and channel resistance

Improved Switch-Level Model



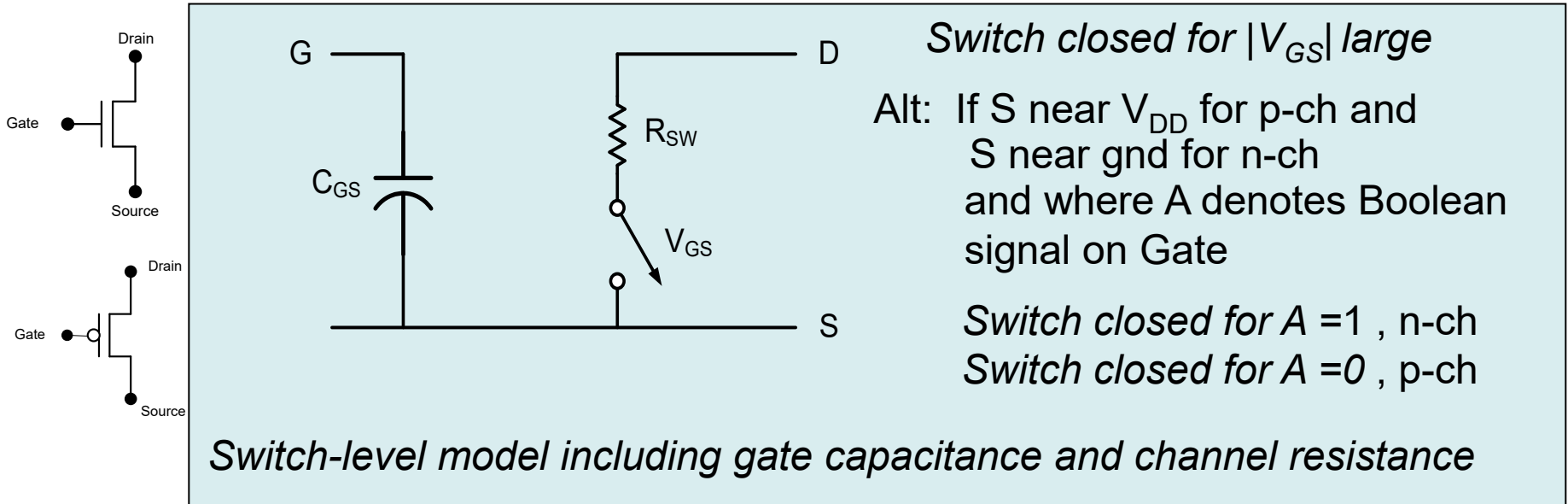
C_{GS} and R_{SW} dependent upon device sizes and process

For minimum-sized devices in a 0.5u process with $V_{DD}=5V$

$$C_{GS} \cong 1.5\text{fF} \quad R_{sw} \cong \left. \begin{array}{l} 2\text{K}\Omega \text{ n-channel} \\ 6\text{K}\Omega \text{ p-channel} \end{array} \right\}$$

Considerable emphasis will be placed upon device sizing to manage C_{GS} and R_{SW}

Improved Switch-Level Model



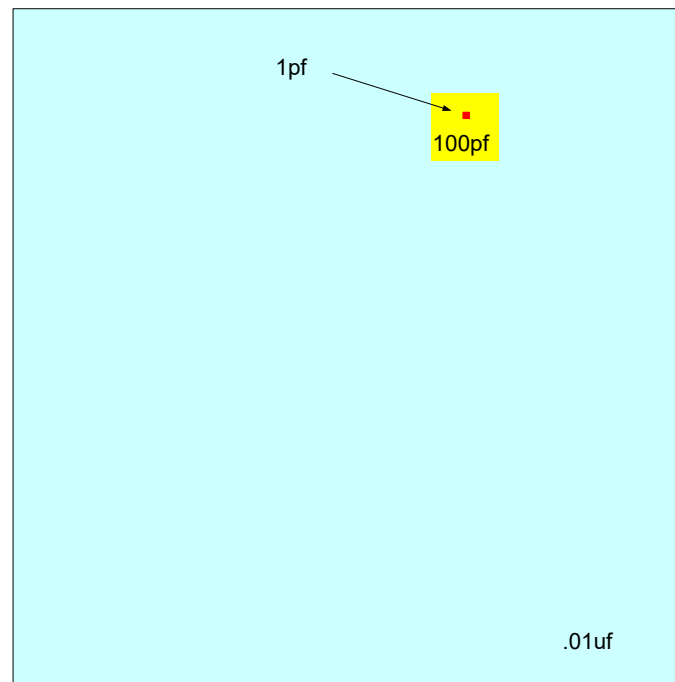
C_{GS} and R_{SW} dependent upon device sizes and process

Will assume for minimum-sized devices in a 0.18u process with $V_{DD}=2V$

$$C_{GS} \cong 1.5\text{fF} \quad R_{sw} \cong \left. \begin{array}{l} 2\text{K}\Omega \text{ n-channel} \\ 6\text{K}\Omega \text{ p-channel} \end{array} \right\}$$

Considerable emphasis will be placed upon device sizing to manage C_{GS} and R_{SW}

Is a capacitor of 1.5fF small enough to be neglected?

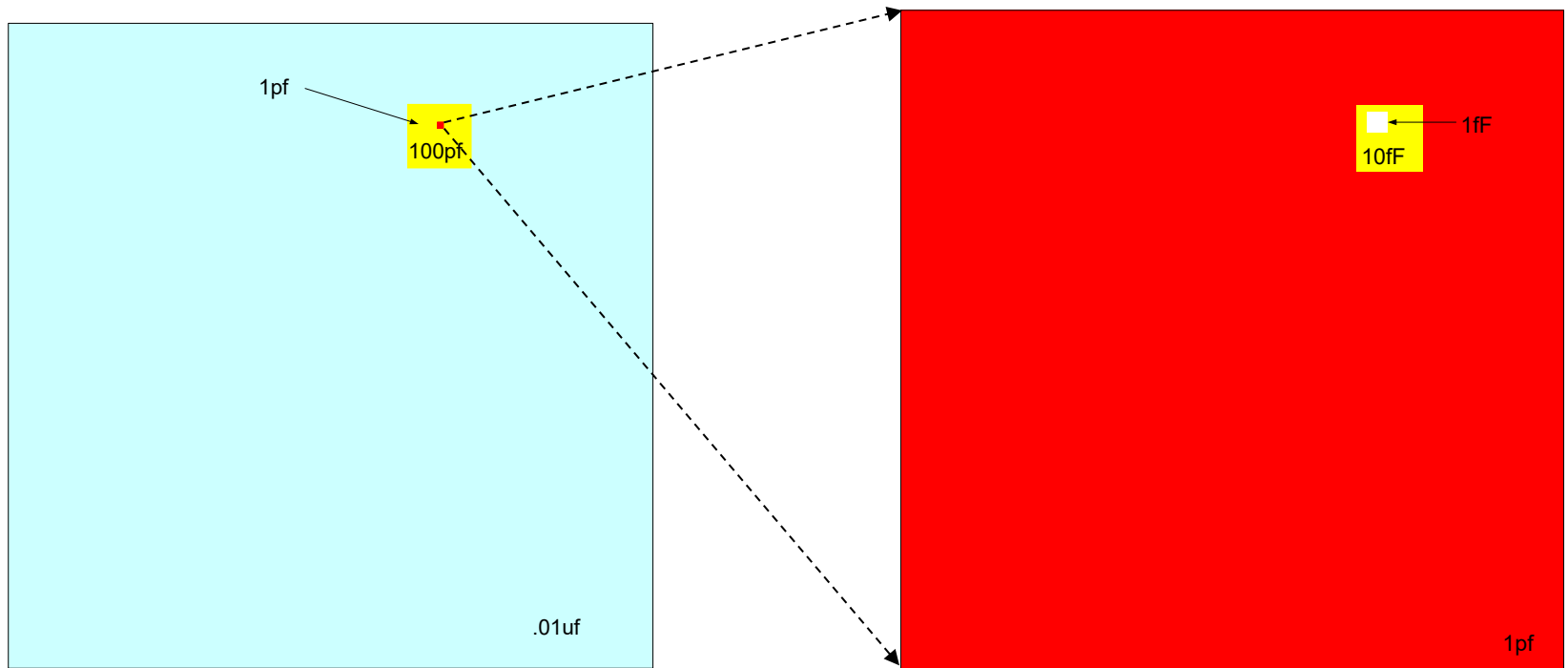


From EE 201 Parts Kit

Capacitors (Farads)		
100p	3	
470p	3	
0.001u	3	2
0.0047u	3	2
0.01u	3	
0.047u	3	
0.1u	3	1
0.47u	3	
1u	3	
10u	3	
100u	3	

Area allocations shown to relative scale:

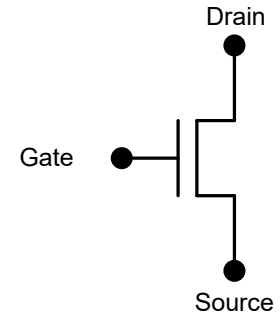
Is a capacitor of 1.5fF small enough to be neglected?



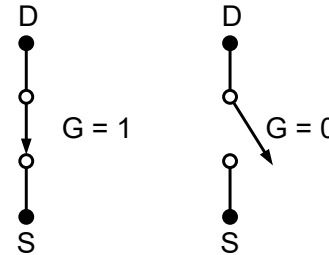
Area allocations shown to relative scale:

- Not enough information at this point to determine whether this very small capacitance can be neglected
- Will answer this important question later

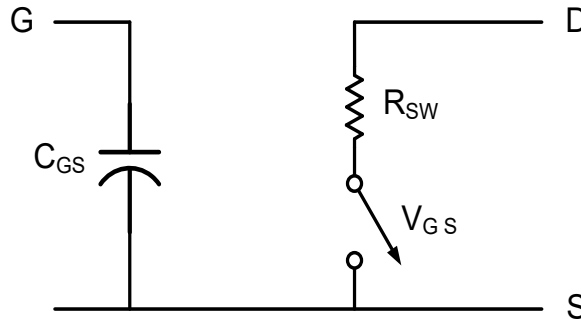
Model Summary (for n-channel)



1. Switch-Level model



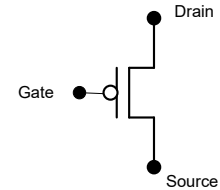
2. Improved switch-level model



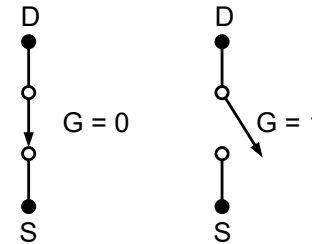
Switch closed for $V_{GS} = \text{large}$
Switch open for $V_{GS} = \text{small}$

Other models will be developed later

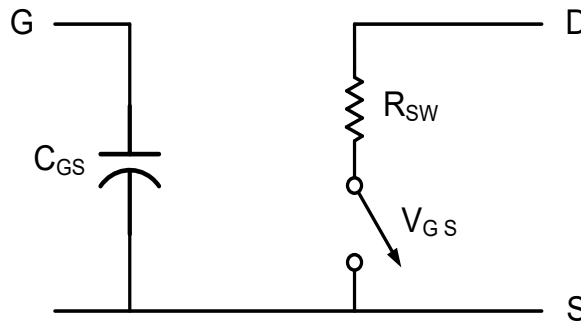
Model Summary (for p-channel)



1. Switch-Level model



2. Improved switch-level model



Switch closed for $|V_{GS}| = \text{large}$
Switch open for $|V_{GS}| = \text{small}$

Other models will be developed later



Stay Safe and Stay Healthy !

End of Lecture 6